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An Improved DFR Control Topology for Single-Phase PV Quasi-Z-Source Inverter with Reduced Capacitance

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Abstract

In single-phase photovoltaic (PV) system, there is double-frequency power mismatch existed between the dc input and ac output. The double-frequency ripple (DFR) energy needs to be buffered by passive network. Otherwise, the ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, electrolytic capacitors are usually used for this purpose due to their high capacitance. However, electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. In this paper, a capacitance reduction control strategy is proposed to buffer the DFR energy in single-phase Z-source /quasi-Z-source inverter applications. Without using any extra hardware components, the proposed control strategy can significantly reduce the capacitance requirement and achieve low input voltage DFR. Consequently, highly reliable film capacitors can be used. The increased switching device voltage stress and power loss due to the proposed control strategy will also be discussed. A 1kW quasi-Z-source PV inverter using gallium nitride (GaN) devices is built in the lab. Experimental results are provided to verify the effectiveness of the proposed method.

Keywords: *Photovoltaic (PV) systems, Gallium nitride (GaN) devices, Double-frequency ripple (DFR), capacitors, Z-source /quasi-Z-source*

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INTRODUCTION

The voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) has been considered for photovoltaic (PV) application in recent years [1-13]. These inverters feature single-stage buck-boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1-5]. The single phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance [6-12]. In three-phase applications, the Z-source (ZS)/ quasi-Z-source (qZS) network only needs to be designed to handle the high frequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is shown in Fig. 1. Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency. The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper.

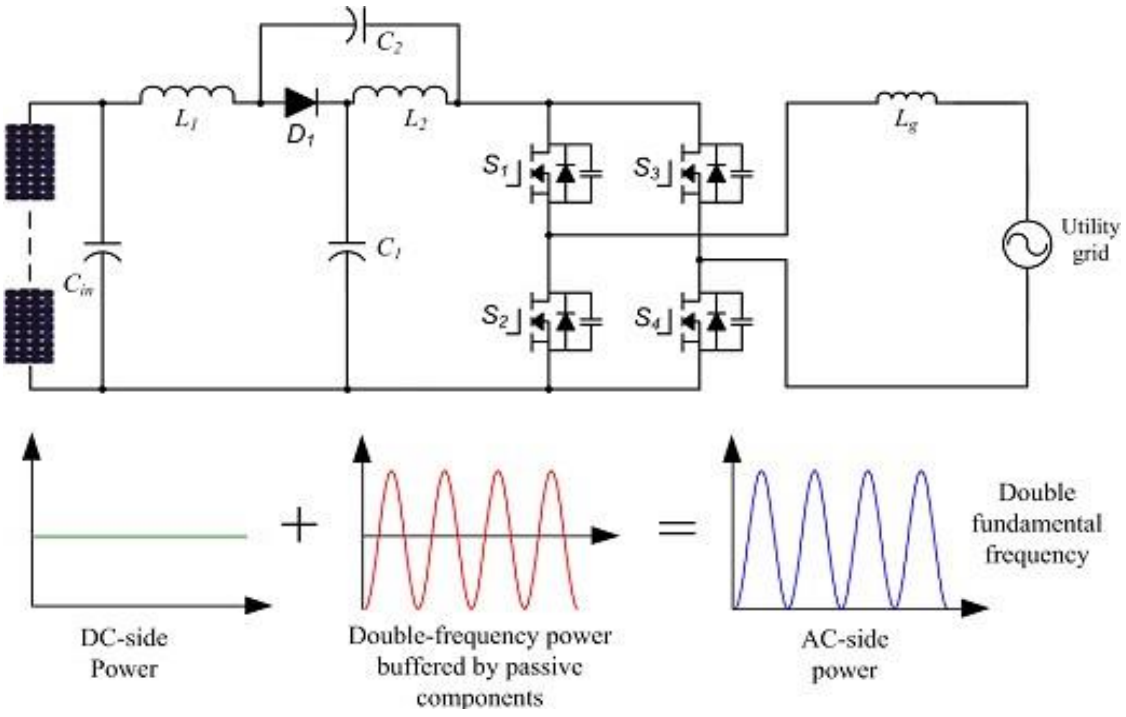


Figure 1: Diagram of a single-phase qZSI based PV system.

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In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which has higher voltage rating than C2.

The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance.

As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion this process is accelerated with higher temperature, eventually leading to performance degradation over time [14]. Therefore, electrolytic capacitors are considered to be the weak component regarding to lifetime, especially under outdoor operation conditions.

Accurate analytical models to calculate the DFR for qZSI have been developed in [8, 15, 16] and the design guidelines for selecting the capacitance to limit the DFR are also provided. Nevertheless, the required capacitance is still large. In [17], two additional smoothing-power circuits are employed to reduce the DFR of DC-link voltage in ZSI.

However, the added circuits increase the system cost and complexity. In [18], a low-frequency harmonic elimination PWM technique is presented to minimize the double frequency ripple on Z-source capacitors. However, the method is used for application with constant voltage input source and double-frequency ripple current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels.

In some reported single-phase two-stage system which is composed of a dc-dc converter and H-bridge inverter, the dclink capacitance can be significantly reduced by using dedicated control [14], [19]. However, the qZSI does not have the dc-dc stage, so the reported capacitance reduction methods cannot be applied in the qZSI.

In this paper, a new control strategy is proposed for ZSI/ qZSI to mitigate the input DFR without using large capacitance, which enables us to use the highly reliable film capacitors. There is no

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extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. In order to apply the capacitance reduction method, it is necessary to study the impact of decreasing the capacitance on system design and performance.

This will be covered in section III. A 1kW qZSI inverter prototype with the proposed control strategy is built in the laboratory. The gallium nitride (GaN) devices are applied in the inverter to increase the system efficiency at high switching frequency. Finally, experimental results are provided to verify the effectiveness of the proposed control system.

PROPOSED CONTROL SYSTEM FOR CAPACITANCE REDUCATION

The basic principle of the proposed capacitance reduction method can be explained by (1).

$$\Delta E = \frac{1}{2} C \left(v_{C_\max}^2 - v_{C_\min}^2 \right) \quad (1)$$

where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and vC_max and vC_min are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE . One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor.

Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented.

In conventional single-phase qZSI, the modulation strategy is shown in Fig. 2(a). The two phase legs of the full bridge are modulated with 180o opposed reference waveforms, m and , m , to generate three-level voltage output. Two straight lines *p v and * vn are used to generate the shoot through duty ratio. When the triangular carrier is greater than v*p or the carrier is smaller than * vn , all four switches S1 − S4 turn on simultaneously for shoot-through.

In the proposed control system, the shoot-through control lines * v p and vn* are

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modified to a line with doublefrequency component as shown in Fig. 2(b). By doing so, the dc side and the qZS capacitor DFR can be decoupled.

An input DFR suppression controller is added in the control system to generate the double-frequency component in v*p and * vn .

Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, gridconnected current controller, qZS capacitor voltage controller and input DFR suppression controller. The MPPT controller provides the input voltage reference vIN*. The error between vIN * and vIN is regulated by a PI controller and its output is the magnitude of the grid current reference.

The grid current ig is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency. The qZS capacitor voltage is regulated by controlling dSH.

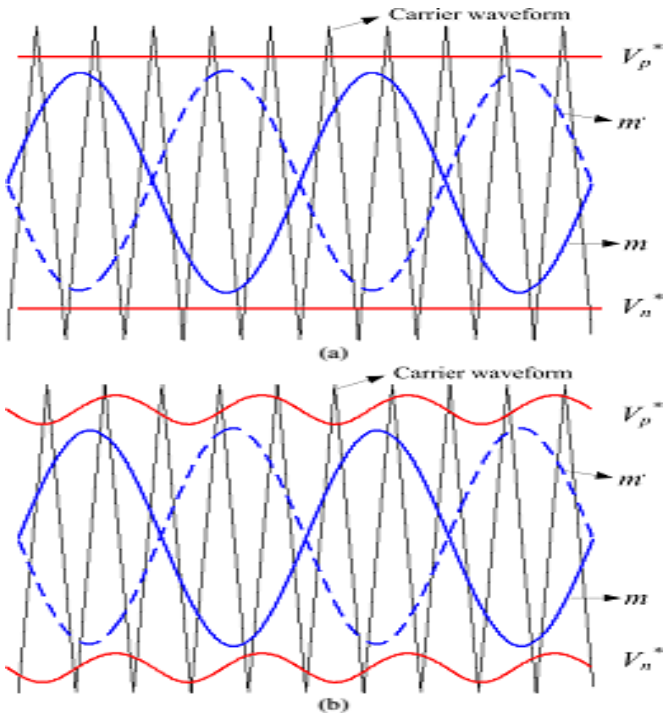


Fig. 2. The modulation strategy of (a) traditional method and (b) proposed method.

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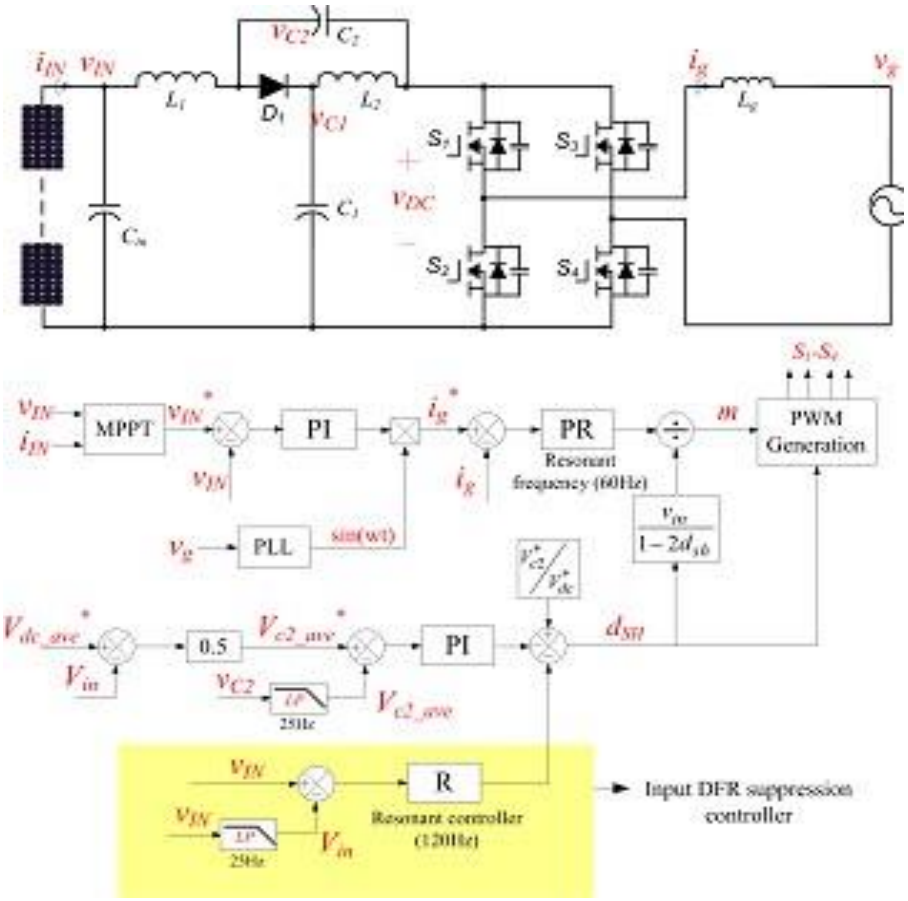


Fig. 3. Diagram of the proposed control system

The shoot through lines can be generated as v p * =1- dSH and vn*=-1+ dSH. It is noted that vC2 is used for the capacitor voltage control. This is because vC2 signal will be used for the qZS network oscillation damping. As will be explained in Section III.A, the oscillation is mainly caused by the resonance among the C2 and inductors. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and vC2 information is required for the implementation. Due to the limited space, the detail of the active damping is not presented in this paper and will be covered in future paper. The vC2 voltage controller only regulates the average value of vC2, which is Vc2_ave, due to the low-pass filter in the signal feedback with a cutoff frequency of 25Hz.

Therefore, the capacitor voltage controller has limited influence on double frequency component and most DFR energy can be kept in qZS capacitors. The reference Vc2_ave* is synthesized using the reference value of the average dc link voltage, Vdc_ave*, and the input voltage

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average value Vin. Vdc_ave* should be selected carefully so that the value of dSH does not become negative because of the double-frequency swing, and the summation of dSH and m is always smaller than 1.

For different input voltages, Vdc_ave* could be optimized to achieve lowest switching device voltage stress. Selection of Vdc_ave* will be explained in more detail in Section III.B when we discuss the increased voltage stress across the switching devices. A feedforward component Vc2*/ Vdc_ave* is added to the output of the capacitor voltage controller to increase the dynamic performance. The DFR suppression controller is composed by one resonant controller whose frequency is designed at two times the grid frequency. The input of the controller is the DFR existed in vIN. It equals to the difference between vIN and Vin. The input DFR suppression controller ensures that the DFR in C1 and C2 does not flow into the input.

EXPERIMENTAL RESULTS

A 1kW qZSI prototype was built in the lab. The parameters of the qZSI are provided in the Table. I. In the qZSI, the voltage across C1 is higher than the voltage across C2, so C1 is

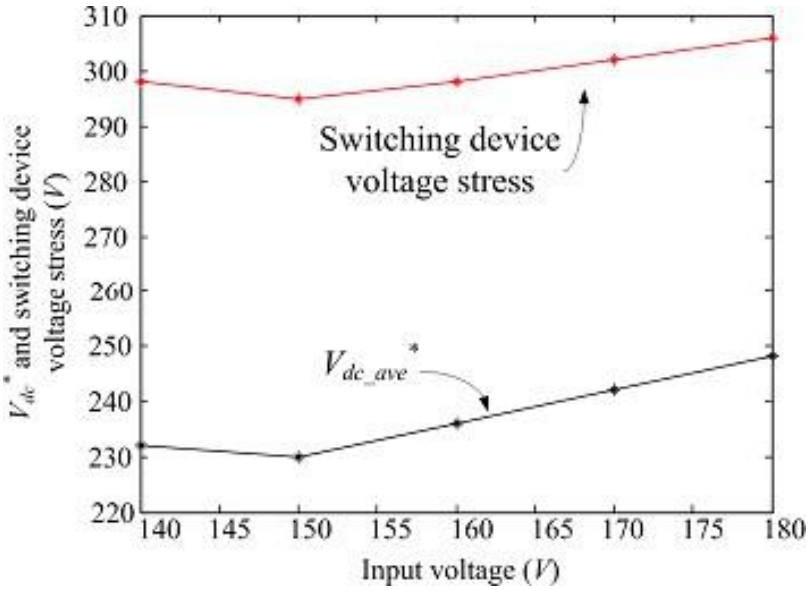


Fig. 5. Vdc_ave* and switching device voltage stress at different input voltages.

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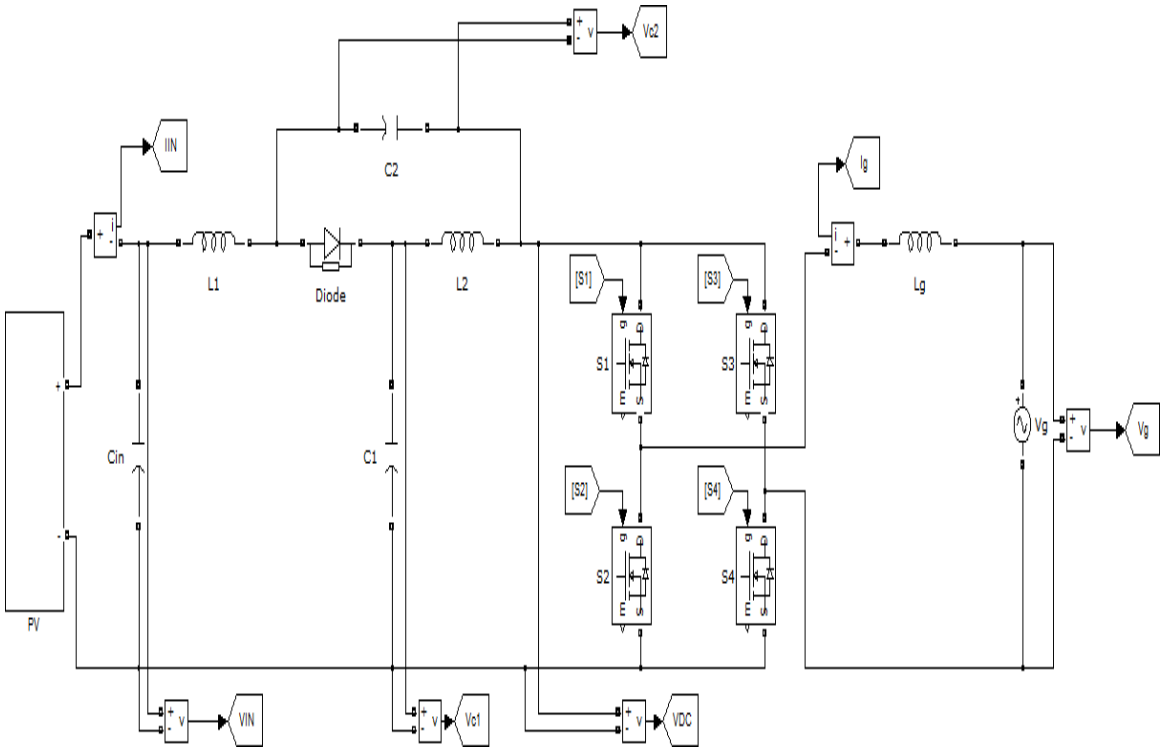


Figure:-6 simulation block diagram of the single-phase qzsi-based PV system.

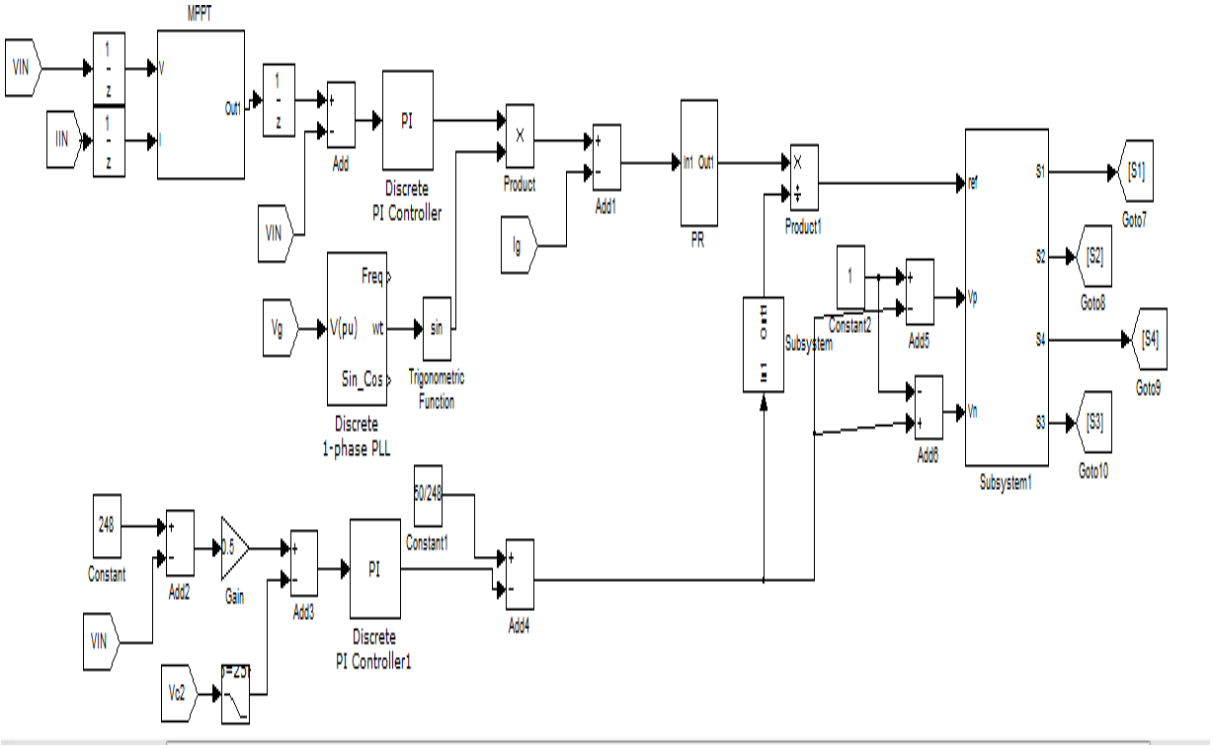


Figure:-7 control block diagram of the single-phase qzsi-based PV system.

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designed to handle the DFR. The quasi-Z-source network design can refer to the model developed in [8]. For the conventional design, in order to achieve 5% voltage ripple at the input side, 2mF capacitor is needed for C1. By utilizing the proposed control strategy, C1 can be reduced to 200μF considering the design trade-off discussed in Section III.B. C2 is designed to limit the high-frequency voltage ripple to 1% of the maximum voltage across C2. The L1 and L2 are designed to limit the high-frequency ripple to 20% of the maximum current through L1 and L2 respectively.

Table I. Parameters of the Qzsi under Study

qZSI Component	Parameters
Input voltage v_{IN}	140-180V
Grid voltage v_g	120Vrms
C_1	2mF for conventional system 200μF for proposed system
C_2	20μF
L_1	330μH
L_2	215μH
L_g	600μH
Switching frequency	100kHz

In conventional design, the maximum switching device voltage stress equals to 200V when VIN=140V. For theproposed method, Vdc* and the switching device voltage stress at different input voltages can be calculated based on the analysis in Section III.B. They are provided in Fig. 5. It is seen that the maximum voltage stress across the switching devices happens at Vin=180V in this design. Vdc_ave* is selected at 248V, so that Dsh_ave is equal to the peak value of Δdsh _dfr . The peak value of vDC, also the switching device voltage stress, is increased to 306V.

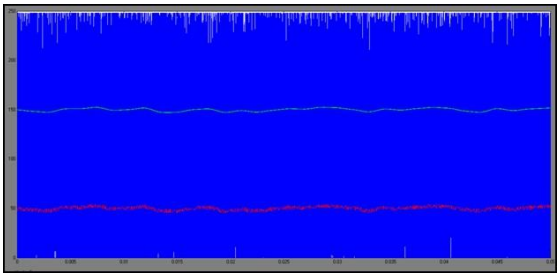


Fig. 7. The vDC, vIN and vC2 waveforms of the qZSI with the conventional control, C1=2mF.

Therefore, the switching device voltage stress is increased by 53% compared with the conventional design. If the grid voltage is increased to 240Vrms, the inverter power rating is kept the same and the input voltage is 260V ~ 340V, and C1 is decreased from 800μF required in conventional design to 100μF with the proposed control, the switching device voltage stress is increased by only 15%. Therefore, there is more benefit to apply the proposed method in qZSI with higher output voltage.

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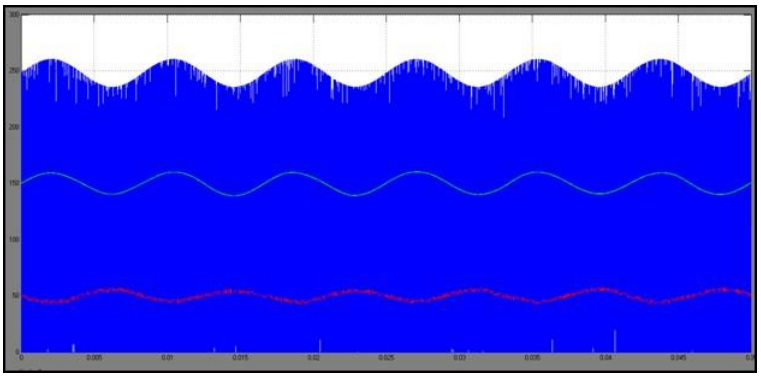


Fig. 8. The vDC, vIN and vC2 waveforms of the qZSI with the conventional control, C1=200µF

The waveforms of vDC, vC2 and vIN for the qZSI system with 2mF capacitor are shown in Fig. 7. The input voltage was 150V and the output voltage was 120Vrms. The inverter was operated at 300W output power condition. The double-frequency components in vDC, vC2 and vIN were 0.72V, 0.336V and 0.774V. The 120Hz ripple in vIN was limited because of the large capacitance. The waveforms for the qZSI with 200µF capacitor, but without the proposed control, are provided in Fig. 8. Because the C1 was significantly reduced, the 120Hz ripples in vDC, vC2 and vIN increased to 7.18V, 2.39V and 5.302V respectively. The distribution of the 120Hz ripple largely depends on the impedance network. The conventional control has minor influence on the ripple distribution. The large 120Hz ripple in vIN could influence the PV energy harvesting. The waveforms of the system with the proposed control strategy are shown in Fig. 9. The 120Hz ripples in vDC, vC2 and vIN were increased to 9.186V, 8.75V and 0.45V respectively. As expected, most 120Hz ripple energy was imposed on C1 and C2. The corresponding output current waveform is shown in Fig. 10 and its total harmonic distortion (THD) value is 4.4%. The efficiency comparison of the conventional qZSI and the qZSI with proposed control at different power outputs is provided in Table. II. As expected in the discussion in Section III.B, because of the increased voltage stress and 120Hz ripple flowing in the qZS network, the efficiencies of the proposed system were around 0.12%-0.69% lower than the conventional system. The C1 capacitance was reduced by 10 times, but with the expense of efficiency decrease. Although the efficiency drop was not significant, it should be considered in the design stage if higher efficiency is desired.

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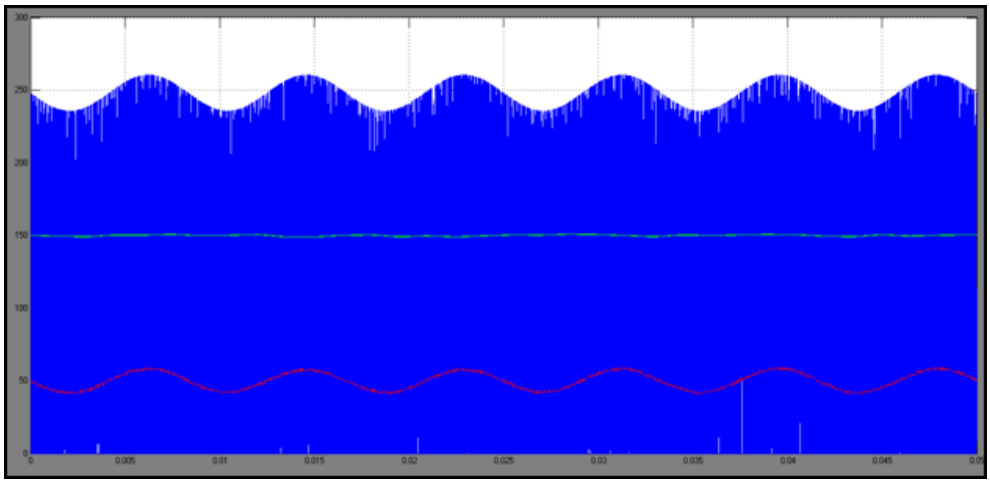


Fig. 9. The vDC, vIN and vC2 waveforms of the qZSI with the proposed control, C1=200µF.

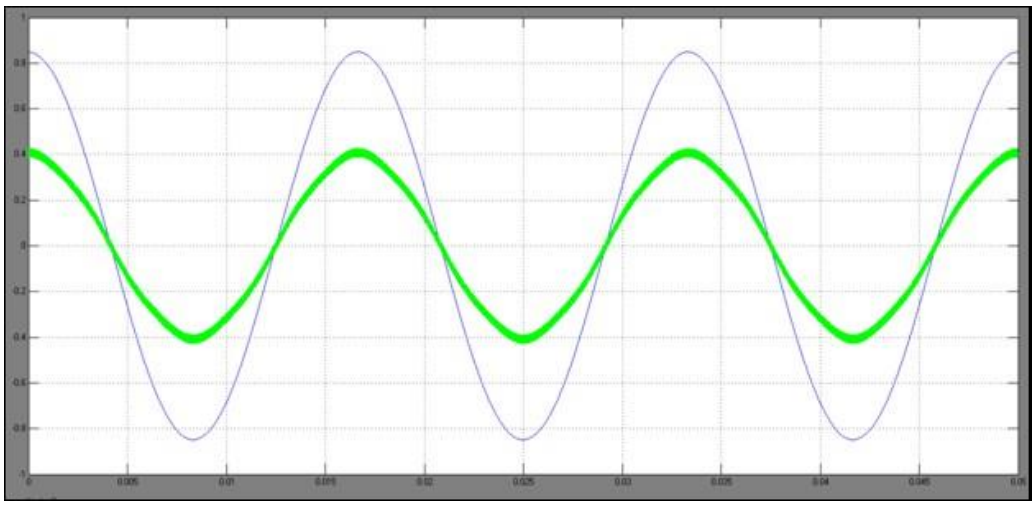


Fig. 10. The output current waveform of the qZSI with the proposed control, C1=200µF.

Table 2. Efficiency Comparison of the Conventional Qzsi and Qzsi with the Proposed Control

	300W	400W	500W	600W
C_1=2mF with conventional control	93.05%	93.18%	93.66%	93.76%
C_1=200μF with proposed control	92.36%	93.06%	93.48%	93.55%

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CONCLUSION

In this paper, a new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the double-frequency ripple energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability much. For the developed 1kW quasi-Z-source PV system, 2mF capacitor can be replaced with a 200μF capacitor by using the proposed method. However, the voltage stress across the switching devices was increased by 53% compared with the conventional design. The efficiency was decreased by 0.12%-0.69% at several selected operation points. It is also shown that there is more benefit if the method is applied for 240Vrms output qZSI. The increase of the switching device voltage stress is only 15% compared with conventional design. This control strategy can also be applied in single-phase ZSI applications.

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