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Investigation and Modeling of the Seven-Levels-Ten Switch Inverter Topology

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Abstract

Multilevel inverters outperform typical two-level inverters due to lower harmonic distortion, less electromagnetic interference, lower common mode voltage, and greater dc link voltages. However, the primary disadvantages of multilayer inverters include sophisticated pulse width modulation management, capacitor voltage balancing, and an increased number of switches. The purpose of this work is to investigate and simulate a single phase seven level inverter design utilising just 10 switches. In addition, two distinct control strategies for a seven-level-ten switch inverter architecture are presented in this study. The R- load is connected to the inverter, and simulation is carried out using the MATLAB/Simulink software.

Keywords: *- Power electronics, Multilevel Inverter, SPWM Techniques*

INTRODUCTION

There has been a significant surge in interest in multilevel power conversion in recent study. Recent research investigations addressed the introduction of new inverter topologies and novel modulation approaches. However, the most popular multi-level inverter topologies are multi-cell inverters [1, 2], diode clamped inverters [3–5], and capacitor clamped inverters [6–8]. Industrial drives, flexible ac transmission systems [7], traction applications in the transportation industry, and grid integration of non-conventional energy sources are some of the uses for these inverters.

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Because all voltage sources have the same value, the seven level-ten switch structure is symmetrical. However, there are numerous asymmetrical topologies that require different voltage sources. This asymmetry necessitates the use of dc voltage sources with a precise relationship between them, as well as a discrepancy in the rating of the semiconductor switches. This research investigates and simulates a novel multilayer inverter design known as reversing voltage (RV) [8]. In comparison to traditional topologies, this topology requires fewer components. It's also more efficient since the inverter includes a component that runs the switching power devices at line frequency. As a result, there is no need for all switches to operate at high frequencies, resulting in simpler and more dependable inverter control. In this study, two alternative control strategies are employed to operate the inverter. The seven level-ten switch inverter architecture simulation results are shown.

SEVEN LEVEL-TEN SWITCH INVERTER

Output voltage is separated into two parts in this hybrid multilevel inverter topology. One part is named “level generator” and is responsible for level generation in positive polarity. High-frequency switches are required in this part to produce required levels. The other part is called “polarity generator” and is responsible for generating the polarity of the output voltage. Polarity generator operates at line frequency. This topology merges the two parts (low frequency & high frequency) to produce the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the level generator (high-frequency part), and then, this part is fed to a polarity generator (full-bridge inverter), which will generate the required polarity for the output. This will reduce number of the semiconductor switches which were responsible to generate the output voltage levels in negative and positive polarities.

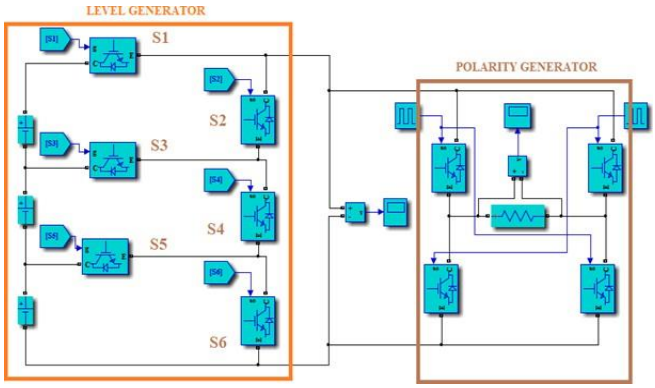


Fig. 1. Seven Level-Ten Switch Inverter or Reversing Voltage Topology

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The number of possible switching states to control the inverter is four. The required output positive voltage levels produced by the level generator are as follows:

1. Zero output level: Switches S2, S4, S6 are ON which short circuits the input of the polarity generator results in the generation of zero voltage.
2. One-third positive output level: Switches S2, S4, S5 are ON, all other high frequency controlled switches are OFF results in the generation of +Vdc/3.
3. Two-third positive output level: Switches S2, S3 are ON, all other high frequency controlled switches are OFF results in the generation of +2Vdc/3.
4. Maximum positive output level: Switch S1 is ON, all other high frequency controlled switches are OFF results in the generation of +Vdc.

SPWM-A CONTROL TECHNIQUE

In order to produce seven levels by SPWM-A control technique, one reference sinusoidal and three triangular carrier signals are required. In this paper, SPWM-A is implemented for its simplicity. Carriers in this method have definite offset from each other and do not have any coincidence. They are also in phase with each other. The reference signal and three carriers for SPWM-A are shown in Fig. 3(a).

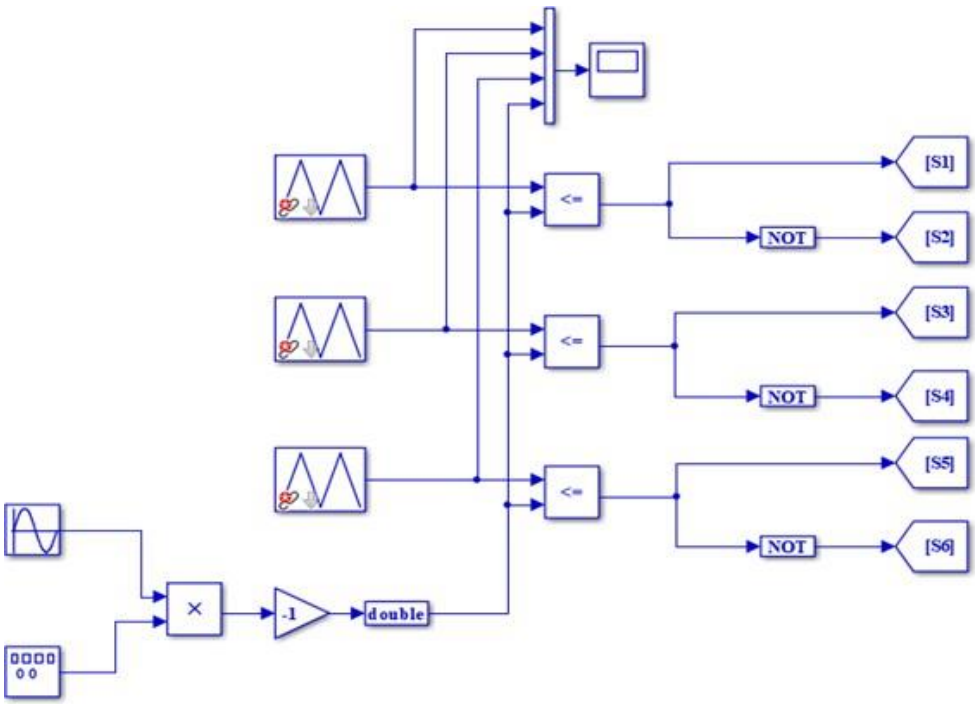


Fig. 2. Simulink model for SPWM-A Technique

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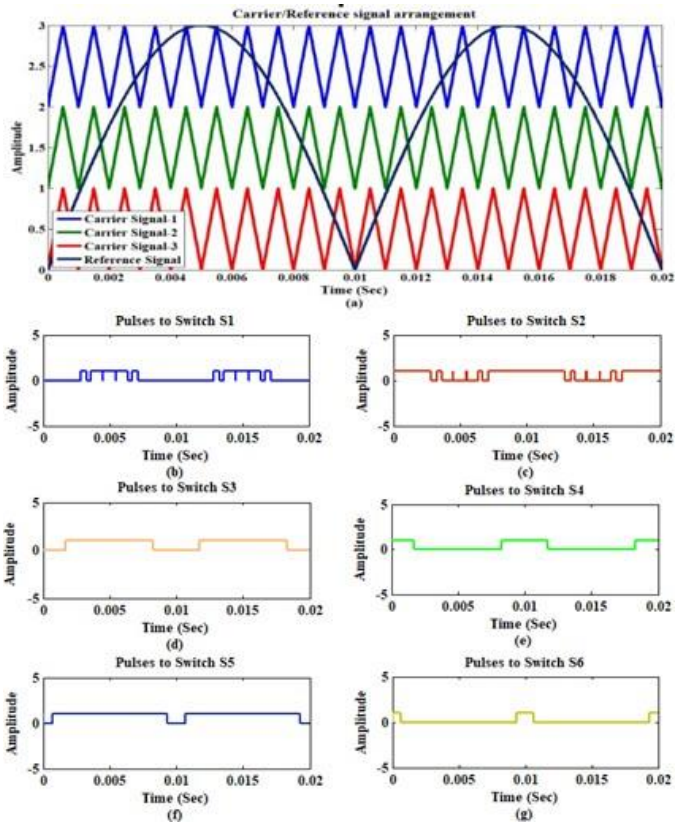


Fig. 3(a)-3(g). Carrier/reference signal arrangement and pulses to switches of seven level ten switch inverter using SPWM-A Technique

4 SPWM-B Control Techniques

The reference signals in the SPWM-B control approach have the same amplitude and frequency as the line frequency. They are phase locked with an offset equal to the amplitude of the carrier signal. Three reference signals will be compared to the carrier signal to create pulses for inverter circuit switches.

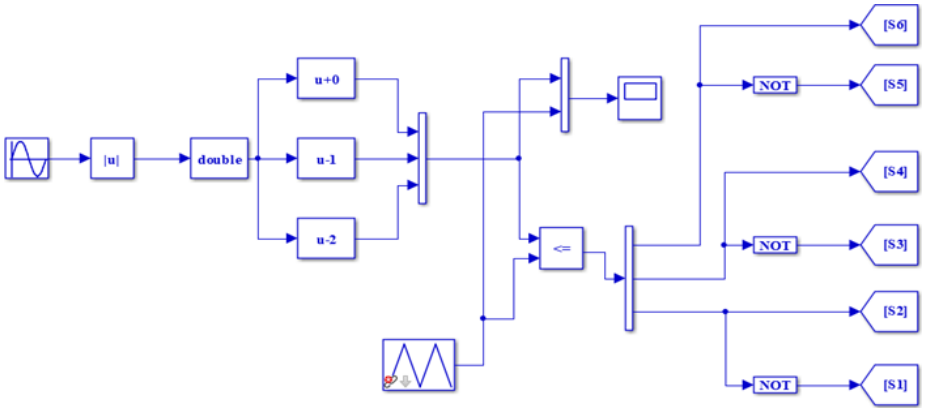


Fig. 4. Simulink model for SPWM-B Technique

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The modulation index for a inverter is defined as the ratio of amplitude of the reference signal to the amplitude of carrier signal. The modulation index for SPWM-B technique is redefined to be M.I.=Ar/(3*Ac),where Ac is peak to peak value of carrier signal and Ar is peak to peak value of the reference signal.

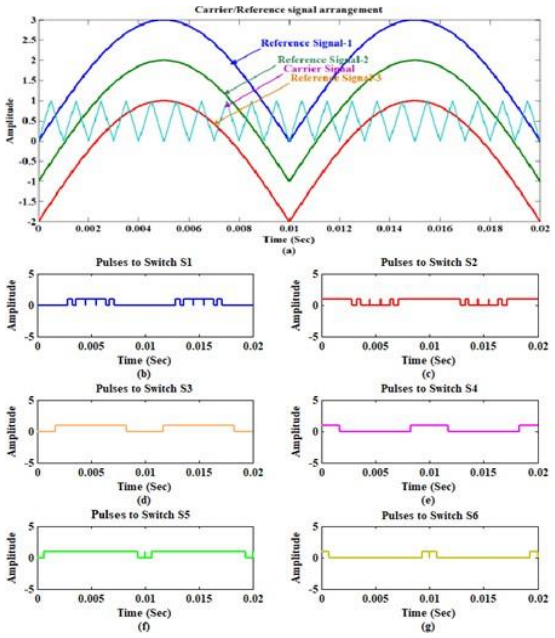


Fig. 5(a)-5(g). Carrier/reference signal arrangement and pulses to switches of seven level ten switch inverter using SPWM-B Technique

SIMULATION RESULTS

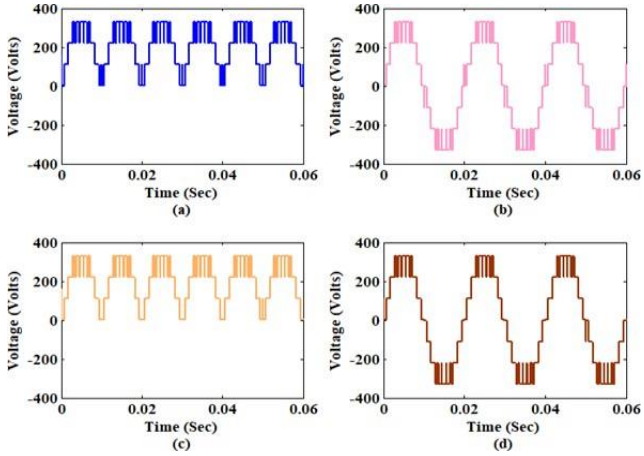


Fig.6. (a) Output voltage waveform of level generator using SPWM-A technique. (b) Output voltage waveform of polarity generator using SPWM-A technique. (c) Output voltage waveform of level generator using SPWM-B technique. (d) Output voltage waveform of polarity generator using SPWM-B technique.

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The seven level-ten switch inverter is simulated using 1000Hz carrier frequency, 50Hz reference frequency, Unity modulation index and value of each voltage source is 110V.Fig.6 (a)-6(d) shows output voltage waveforms of seven level-ten switch inverter using both SPWM-A and SPWM-B techniques.

CONCLUSION

In MATLAB and Simulink software, a seven-level-ten switch inverter is simulated using both SPWM-A and SPWM-B approaches. In terms of the amount of switches required, the control system, and reliability, this inverter design outperforms traditional topologies, providing better output waveforms. The switching action is divided into high and low-frequency components in the aforementioned structure. This improves the converter's efficiency while also lowering the size and cost of the inverter.

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