

A Review on New 7-Level H-Bridge Inverter-Fed Induction Motor with Low Harmonics

Rakesh Singh Kumwat¹, Jayant Kumar²

Associate Professor¹, Student²

Department of Electrical Engineering

A.D. Patel Institute of Technology

Corresponding Author's E-mail:- jayankkumar5@gmail.com²

Abstract

A multilevel structure with more than five layers has the potential to drastically diminish harmonic content. The number of levels increases the output voltage and power. Adding a voltage level necessitates the addition of a primary switching device to each phase.

The objective here is to create the seven-level H-Bridge inverter with the fewest switches possible. This circuit's output is delivered to the induction motor. Using this approach, we can adjust the speed of the induction motor while also reducing noise and vibration. This study focuses on increasing the efficiency of multilayer inverters and the quality of the output voltage waveform. With only seven switches, a new seven-level strategy is implemented. The MATLAB simulation has been completed, and the hardware has been constructed by using IGBTs for the seven switches of the seven-level inverter.

Keywords: - H-Bridge, IGBT, Multilevel inverter, Induction motor

INTRODUCTION

Utility interface systems and motor drives can both benefit from multilevel converters. These converters have a low THD at the output voltage as well as a

high efficiency and power factor. Multilevel converters are classified into three types: diode clamped, flying capacitors, and cascaded. The following are the primary benefits of multilayer

converters: They are suitable for high-voltage and high current applications.

- a) They have higher efficiency since the devices can be switched at a low frequency.
- b) Power factor is close to unity for multilevel inverters used as rectifiers to convert ac to dc.
- c) No Electromagnetic Interference (EMI) problem exists.
- d) No charge unbalance problem results when the converters are in either rectification or inversion mode.

The multilevel converters require balancing the voltage across the series-connected dc bus capacitors. Capacitors tend to overcharge or completely discharge, at which condition the multilevel converter reverts to a three-level converter unless an explicit control is devised to balance the capacitor charge.

The voltage-balancing technique must be applied to the capacitor during the operations of the rectifier and the inverter. Thus, the real power flow into a capacitor must be the same as the real power flow out of the capacitor, and the net charge on

the capacitor over one cycle remains the same.

LITERATURE SURVEY

The research [1] compares two types of approaches or topologies, namely cascaded and reduced switches topologies. This study makes advantage of the reduced switches topology.

The THD contents of 7, 11, and 15 level cascaded multilevel inverters are described in the work [7]. The overall harmonic distortion relies on the switching angles for various units of multilevel inverters; hence, the switching angles are computed first using the Newton-Raphson approach, which eliminates some harmonic components. THD analysis is performed both analytically and numerically utilising the obtained switching angles.

The study [20] shows how to produce lower harmonic distortion with a novel architecture of multilevel inverters.

When compared to typical cascaded H-Bridge multilevel inverters, the novel topology has the benefit of requiring fewer components and may be expanded to any number of levels. The harmonic reduction is achieved here by selecting proper switching angles.

The study [21] examines the seven-level inverter's analysis and simulation. For a seven-level inverter, the % total harmonic distortion is determined. MATLAB is used to verify the operation of the seven-level inverter.

REDUCED SWITCHES SCHEME

The major goal here is to enhance the output voltage quality of the 7-level inverter with fewer switches. One critical aspect of this 7-level inverter design is the elimination of lower order harmonics and the generation of a nearly sinusoidal output voltage waveform. The accurate and meticulous determination of the switching angles for creating the voltage with fundamental frequency is a critical issue in the fundamental switching scheme. This 7-level inverter has three modes of operation.

These modes are described in details as below.

A. POWERING MODE

- This mode of operation occurs when both the load current and voltage have the same polarity. During the positive half cycle, when the output voltage is V_{dc} , the path of flow of current consists of: the lower supply, D6, Q1, load, Q4 and back to the lower supply.
- When the output voltage is $2V_{dc}$, the path of flow of current is: the lower source, Q5, the upper source, Q1, load, Q4 and back to the lower source.
- When the output voltage is $3V_{dc}$, the path of flow of current comprises: upper supply, Q1, load, Q4, Q7, lower supply. During the negative half cycle, the switches Q1 and Q4 are replaced by the switches Q2 and Q3 respectively.

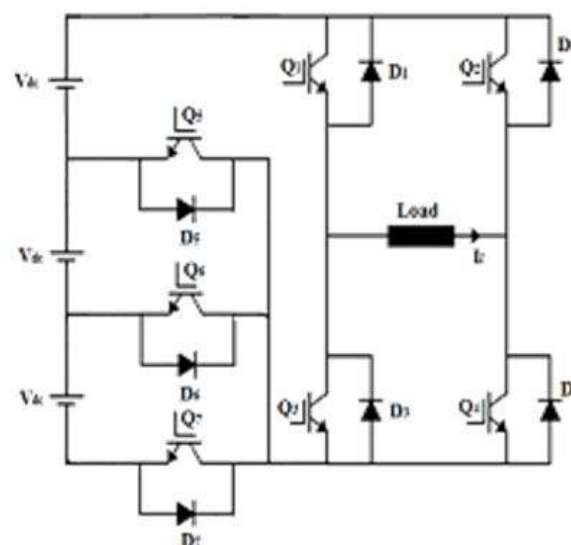


Fig. 1 Power circuit with only 7 switches for 7-level output

Free-wheeling mode occurs when one of the main switches is turned off while the load current needs to continue its flow due to the load inductance. This feature is obtained with the help of anti-parallel diodes across the switches and the load circuit is disconnected from the source terminals.

In this mode of operation, the positive half cycle current flow comprises: Q1, load and D2 or Q4, load and D3. Whereas in the negative half cycle, the current flow path includes: Q3, load and D4 or Q2, load and D1.

C. REGENERATING MODE:

During this mode of operation, part of the energy stored in the load inductance is returned back to the source. This occurs during the intervals when the load current

is negative during the positive half cycle and vice-versa. During this period, the output voltage is zero.

The positive current flow path consists of: load, D2, Q6, the lower source and D3. While the negative current flow path consists of: load, D1, Q6, the lower source and D4.

SELECTIVE HARMONIC ELIMINATION:

The Selective Harmonic Elimination Stepped Waveform (SHESW) technique is suitable for a 7-level inverter circuit. Employing this technique along with the multilevel topology, the low Total Harmonic Distortion (THD) output waveform without any filter circuit is possible.

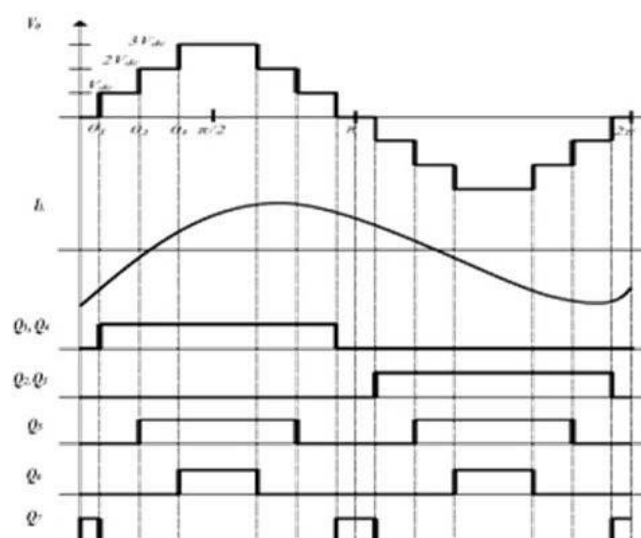


Fig. 2 Waveforms of the 7-level inverter under consideration

(A) FOURIER SERIES AND HARMONICS ELIMINATION THEORY:

After applying Fourier theory to output voltage waveform of multilevel converters, which is odd quarter-wave symmetric, we can find the Fourier expression of multilevel output voltage as given by equation (1). If the DC voltages are equal in multilevel converter, the equation for the fundamental frequency switching control method can be given as:

$$V(t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) (\cos(n\theta_2) + (\cos(n\theta_3) + \dots + (\cos(n\theta_s)) \sin(n\omega t) \quad (1)$$

From this equation, it is seen that the output voltage has no even harmonics because output voltage waveform is odd quarter-wave symmetric. It also can be seen from equation (2) that peak values of these odd harmonics are expressed in terms of the switching angles θ_1 , θ_2 , and θ_s . Also, the harmonic equations produced from (2) are transcendental equations.

Depending on the harmonic elimination theory, if we want to eliminate the n th harmonic, then

$$\cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_s) = 0 \quad (2)$$

That means to choose a series of switching angles to let the value of the n th harmonic be zero. Hence, an equation with 's' switching angles will be used to control the 's' different harmonic values. Generally, an equation with 's' switching angles is used to determine the fundamental frequency value, and to eliminate 's-1' low order harmonics. For an equation with three switching angles, equation (2) becomes

$$V(t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) + (\cos(n\theta_2) + (\cos(n\theta_3)) \sin(n\omega t) \dots \dots \dots (3)$$

(A.) TRANSCENDENTAL EQUATIONS TO SOLVE:

Here, we derived harmonic equations for eliminating the 3rd and 5th order harmonics. The resulting harmonic equations are as follows:

$$\cos \theta_1 + \cos \theta_2 + \cos \theta_3 = \pi V_1 / 4V_{dc} \dots (4)$$

$$\cos 3\theta_1 + \cos 3\theta_2 + \cos 3\theta_3 = 0 \dots \dots \dots (5)$$

$$\cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 = 0 \dots \dots \dots (6)$$

To simplify the expression, equation (4) can be written as

$$\cos \theta_1 + \cos \theta_2 + \cos \theta_3 = m \dots \dots \dots (7)$$

$$\text{where } m = \pi V_1 / 4V_{dc} \dots \dots \dots (8)$$

These harmonic equations (4) to (6) are transcendental equations. They are

difficult to solve without using some type of numerical iterative technique. Here Newton Raphson method is employed for solving these equations.

(C) SOLVING THE HARMONIC EQUATIONS USING NEWTON RAPHSON METHOD:

To solve the harmonic equations by resultant theory, they must be changed into polynomials. First, we change the variables,

$$x_1 = \cos(\theta_1) \quad (9)$$

$$x_2 = \cos(\theta_2) \quad (10)$$

$$\text{and } x_3 = \cos(\theta_3) \quad (11)$$

Also, use the following trigonometric identities:

$$\cos 3\theta = 4\cos^3(\theta) - 3\cos(\theta) \quad (12)$$

$$\cos 5\theta = 5\cos\theta - 20\cos^3\theta + 16\cos^5\theta \quad (13)$$

Then, apply them to the transcendental harmonic equations above, and the following polynomial harmonic equations can be found.

For the fundamental frequency harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^3 (x_n - m) = 0 \quad (14)$$

For the 3rd harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^3 (4x_n^3 - 3x_n) = 0 \quad (15)$$

For the 5th harmonic:

$$P_1(x_1, x_2, x_3) = \sum_{n=1}^3 (5x_n^5 - 20x_n^3 + 20x_n) = 0 \quad (16)$$

The polynomial equations can be solved by using the Newton Raphson method. The following are steps for solving the equations. Substitute the initial guesses for variables. Then form the jacobian matrix with Newton's formula. Repeat the same steps until the solutions to converge. Thus, the switching angles θ_1 , θ_2 and θ_3 are obtained as follows:

$$\theta_1 = 8.766^\circ$$

$$\theta_2 = 28.688^\circ$$

$$\theta_3 = 54.939^\circ$$

From the fig. 2, the switching patterns for switches Q1 to Q7 become clear. Here, the fundamental frequency switching scheme is employed, which drastically reduces the switching losses.

Switching losses are directly proportional to the switching frequency. In this method the switching frequency is less as compared to the other methods and hence the switching losses are less which is a bigger advantage.

CIRCUIT DIAGRAM

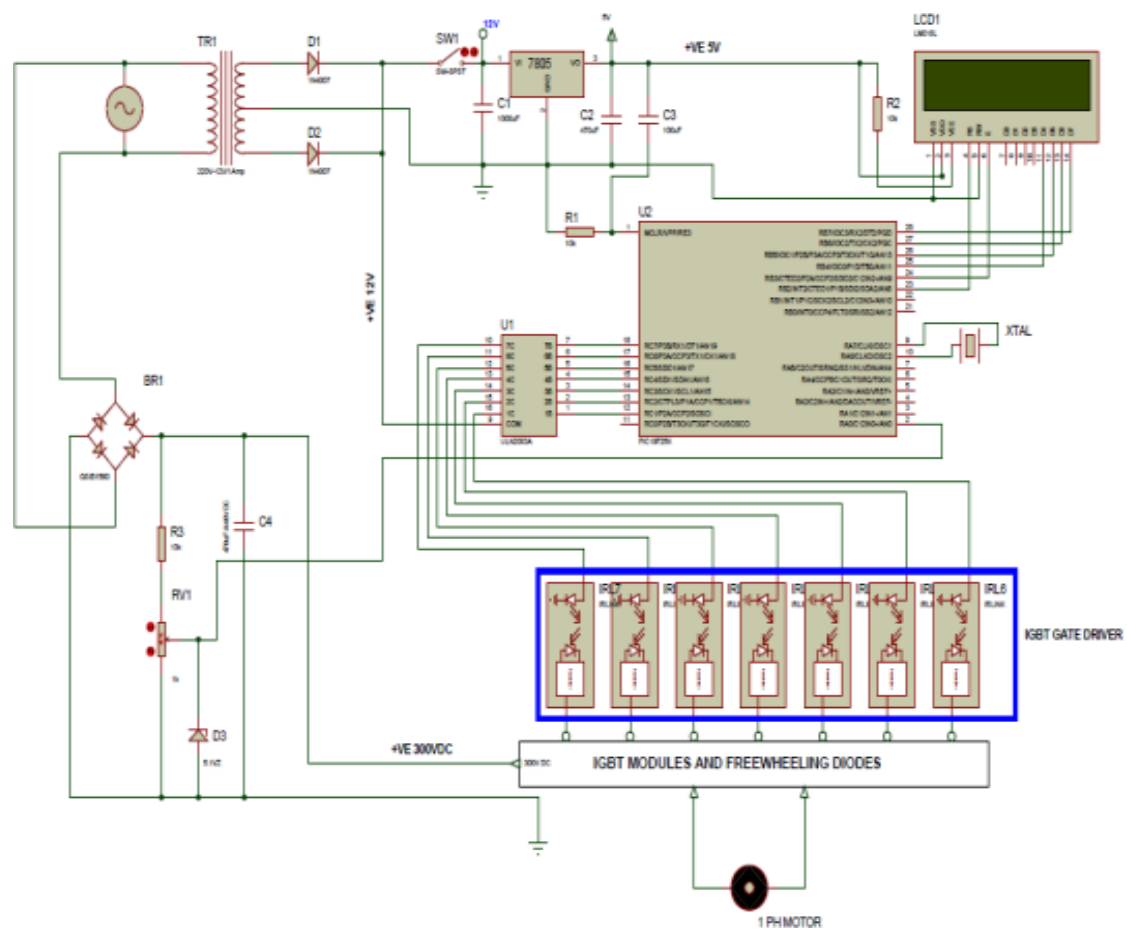


Fig. 4 Overall circuit diagram of the complete arrangement for single phase structure

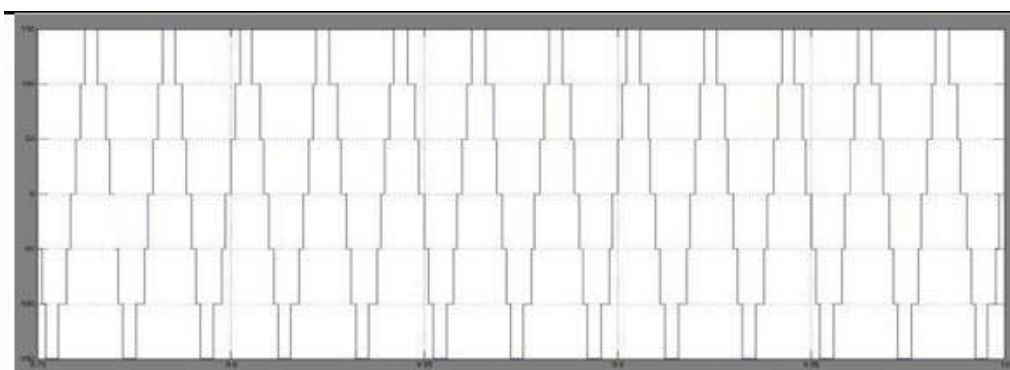


Fig. 5 Output voltage for single phase 7-level inverter

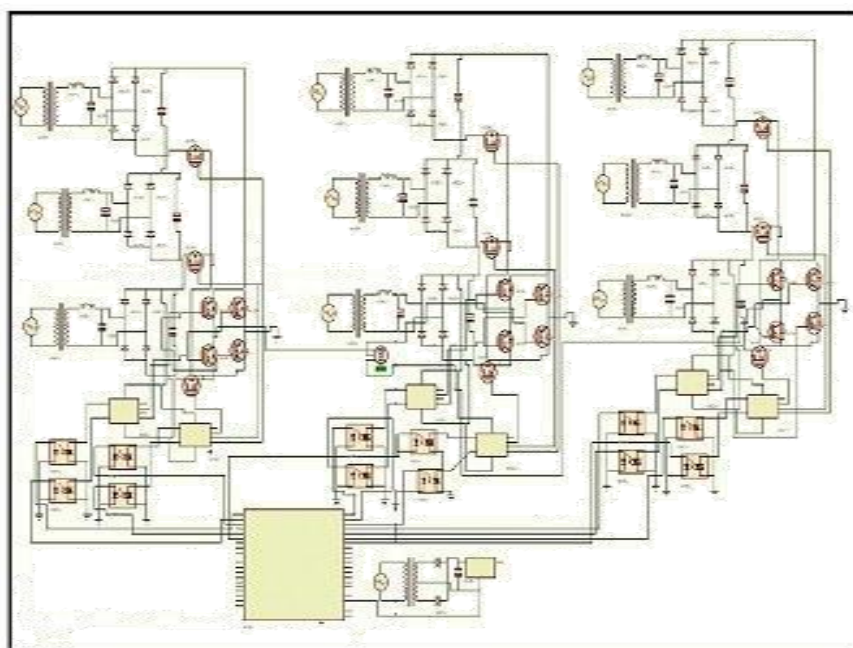


Fig. 6 3-phase Structure for the scheme for 7-level inverter

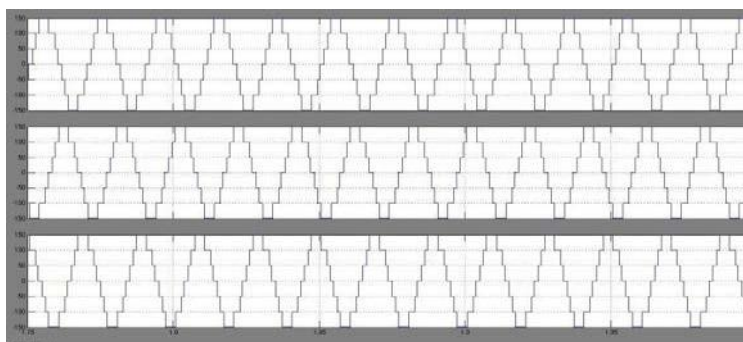


Fig.7 Phase to ground voltage for 3- Phase 7- Level Inverter

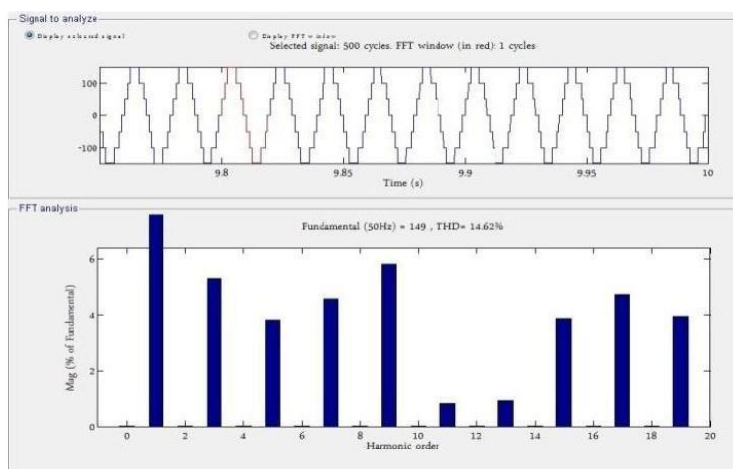


Fig. 8 FFT Analysis

COMPONENTS AND THEIR FUNCTIONS

A. PIC MICROCONTROLLER

1. PIC (Peripheral Interface controller) Microcontrollers are specialized microcontroller chips produced by micro- chips Technology in Chandler, Arizona.
2. The main function of the PIC microcontroller is to govern the operation of embedded systems in motors, vehicles, robots etc.
3. PIC16F887 Microcontroller is used in the hardware circuit.
4. The operating frequency of PIC is 0-20 MHz.
5. The required power supply for the PIC is 2.0 to 5.0 volts.

B. IGBT DRIVER

1. An IGBT driver is a semiconductor chip which is used as a switch or rectifier in power electronic circuit.
2. Switches are used in order to break or divert a circuit.
3. There are 7 IGBT drivers used in this implementation.

4. The input supply and output ranges between 12-24 volts.

5. IGBT driver consists of opto-coupler and voltage amplifier.

C. IGBT SWITCH

1. It is a 3 terminal power semiconductor device with 4 alternating layers (P-N-P-N) and primarily it is used as an electronic switch.
2. The rating of each IGBT switch is 12 amperes and 7 IGBT switches are used.
3. It switches electric power in many modern appliances.
4. It is designed to turn on and turn off rapidly.

D. DRIVER INTERFACING IC

It is used for microcontroller and driver short circuit protection.

E. CRYSTAL OSCILLATOR

A crystal oscillator is an electronic oscillator circuit which uses the mechanical resonance of vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency.

F. HEAT SINK:

It is a substance or device for absorbing unwanted or excessive heat from IGBT and cools it down.

EXPERIMENTAL SETUP:

The last four IGBT's are connected in such a manner so as to form an H-Bridge. The

output of the circuit is taken from this H-Bridge and is fed to the load.

An induction motor is used as a load which gives a smooth running and an operation free of noise and vibrations.

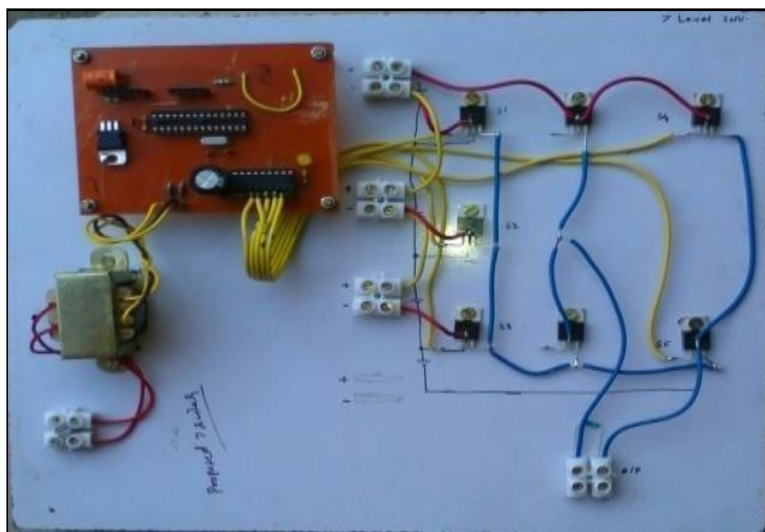


Fig. 9 Experimental setup of the 7-level inverter circuit



Fig. 10 Complete assembly of the experimental setup of 7-level inverter with output waveform

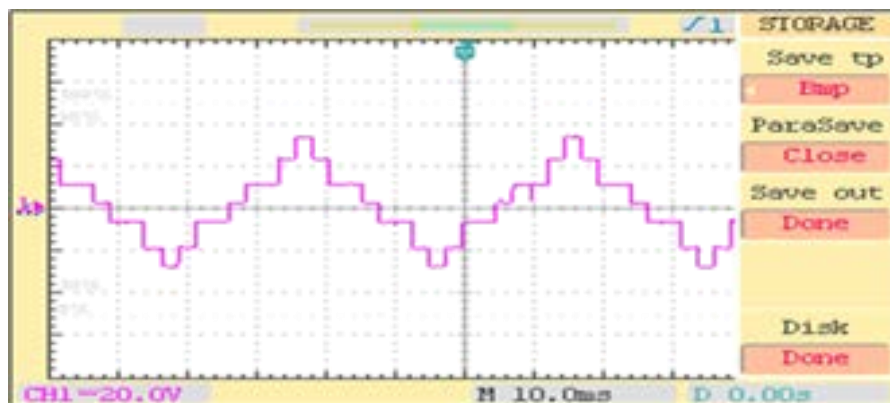


Fig. 11 Output voltage waveform for B phase for the 7-level inverter as seen on Digital Storage Oscilloscope (DSO).

APPLICATIONS

There is a lot of interest in using voltage source inverters in high-power applications such as utility systems for regulated reactive power sources. An inverter can provide a regulated reactive current and function as a static volt-ampere reactive (VAR) compensator in steady-state operation (STATCOM). These inverters can also lower the physical size of the compensator while improving its effectiveness during power system outages.

The most common applications of multilevel converters include

1. Reactive power compensation,
2. Back to back intertie, and
3. Variable speed drives.

Other applications include:

1. The inverter banks are used in big industries.
2. They are used in electric traction.
3. It is used in pump, fan, mills, chemical industries, etc.
4. It is used in electric and hybrid power trains.
5. CSI and VSI fed drives are nowadays largely used in the industries for power quality improvement purposes.
6. They are used in variable speed drive applications.

CONCLUSION

1. We may minimise the number of switches necessary by implementing the new multilayer inverter method.
2. It lowers capital costs and complexity.
3. Despite the fact that 7 switches are required, the above-calculated switching angles 1, 2, and 3 are

sufficient for this circuit. This is plainly seen in fig. 2.

4. This technique is applicable to any number of levels.
1. Using this innovative approach, a 7-level output phase voltage and a 9-level output line voltage are generated with reduced total harmonic distortion (THD).
5. Speed control over a wide range is possible.
6. The suggested technique has the benefit of fewer switches and lower harmonics, with a THD value of 14.62% at 149V. The harmonic spectrum of the simulation system for the suggested strategy is given in fig. 8, indicating that the results are well within the stipulated limitations of IEEE standards.

REFERENCES

1. Hossein Sepahvand, Jingsheng Liao and Mehdi Ferdowsi, "Investigation on capacitor voltage regulation in cascaded H-Bridge multilevel converters with fundamental frequency switching," IEEE
2. Transactions on Industrial Electronics, Volume-58, Number-11, pp 5102-5111, 2011.
3. J. Napoles, A.J.Watson, J.J.Padilla, J.I.Leon, L.G.Franquelo, P.W.Wheeler and M.A. Aguirre, "Selective harmonic mitigation Technique for cascaded H-Bridge converters with non-equal DC link voltages," IEEE Transactions on Power Electronics, pp 1-9, 2012.
4. Dr. Jagdish Kumar, " THD analysis for different levels of cascade multilevel inverters for industrial applications," International Journal of Emerging Technology and Advanced Engineering. Website: www.ijetae.com (ISSN: 2250-2459, Volume-2, Issue-10, October 2012).
5. Maheswari, S. Mahendran, Dr. I.Gnanambal, "Implementation of fundamental frequency switching scheme on multilevel cascaded H-Bridge inverter fed three phase induction motor drive," Wulfenia journal, Klangfurt, Austria, Volume-19, Number-8, pp 10-24,2012.
6. Tom Wanjekeche, Dan Valentin Nicolae and Adisa Abdul Jimoh, "Realization of a nine-level cascaded NPC/ H-Bridge PWM inverter using phase shifted carrier PWM," Journal of Energy and Power Engineering 6 (2012) 1335-1342.

7. M. Jagabar Sathik, K. Ramani, "A novel approach of multilevel inverter with reduced power electronics devices," International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, Volume-8, Number-11, 2014.
8. Gobinath. K, Mahendran. S, Gnanambal. I, "New cascaded H-bridge multilevel inverter with improved efficiency," International Journal of advanced research in Electrical, Electronics and Instrumentation Engineering, Volume 2, Issue 4, April 2013 (www.ijareeie.com).
9. O. Chandra sekhar, K. Chandra sekhar, "Modulation and control of multilevel inverter fed DTC induction motor drive," International Journal of Energy and Power (IJEP), Volume-1, Issue-1, August 2012, pp 7-17.
10. Bharath K., R.J.Satputaley, "Single phase assymetrical cascaded multilevel inverter design for induction motor," International Journal of Electrical, Electronics and Data communication, ISSN: 2320-2084, Voume-1, Issue-3.
11. Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad azem Bakhshizadeh, Naeem Farokhnia and S.Hamid Fathi, "Application of the BEE algorithm for selective harmonic elimination strategy in multilevel inverters," IEEE Transactions on Power Electronics, Volume-27, Number-4, pp 1689-1696, 2012.
12. M. Murugesan R. Sakthivel, E. Muthukumaran and R. Sivakumar, "Sinusoidal PWM based modified cascaded multilevel inverter," International Journal of Computational Engineering Research (IJCER), ISSN: 2250-3005, March-April 2012, Volume-2, Issue-2, 529- 539.
13. K. Mahendran, Dr. S.U. Prabhu, "An Experimental investigation on implementation of advanced cascaded multilevel inverter for Renewable Energy applications," International Journal of Innovations in Engineering and Technology (IJIET), ISSN: 2319-1058, Volume-7, Issue-1, 2016.
14. R. Kavitha, Dr. Rani Thottungal, Rini Gloria. C, "Hardware implemetation of hybrid cascaded multilevel inverter for generating different voltage levels," International Journal of Emerging Technology and Advanced

Engineering (IJETAE), ISSN:
2250-2459, Volume-4, Issue-3,
March-2014.

15. Nayna Bhargava, Sanjeev Gupta, S. P. Phulambrikar, "Analysis of assymetrical cascaded 7 level and 9 level multilevel inverter for design for asynchronous motor," International Journal of Engineering Research and Technology (IJERT), ISSN: 2278-0181, Volume-3, Issue-8, August-2014.
16. Atithi B. Patel, Hiren H. Patel, "Control of assymetric cascaded H-Bridge multilevel inverter," International Journal of Current Engineering and Scientific Research (IJCESR), ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, Volume-2, Issue-7, 2015.