

Modular Multilevel Cascaded Inverter Based on Capacitor Voltage Balancing Control using Carrier Phase Shifted Sinusoidal Pulse Width Modulation Technique

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Abstract

This paper presents a control strategy for voltage balancing of the capacitors of different sub-modules in single phase five-level modular multilevel cascaded inverter based on carrier phase-shifted sinusoidal pulse width modulation. Since the modules consist of capacitors, whose voltages can vary significantly throughout the operation of the converter, the need for a balancing algorithm is derived. Through the specific algorithm it is being ensured that all the capacitors are kept on the same voltage level and all the power devices are equally stressed. Thus the combination of averaging and balancing control enables the modular multilevel converter to achieve the voltage balancing of the sub-module capacitors. The simulation has been carried out using MATLAB/Simulink and the effectiveness of the voltage-balancing control is confirmed based on simulation results.

Keywords: Modular Multilevel Cascaded Inverter (MMCI), Double star chopper cells (DSCC), Carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM), Total harmonic distortion (THD), Fast Fourier Transform (FFT)

I. INTRODUCTION

Modular multilevel converters have great potential in high-power applications, such as dc interconnections, dc power grids, and off-shore wind power generation are in need of accurate power flow control and high-efficiency power conversion in order to reduce both their operating costs and their environmental impact [1]. High power converters for utility applications require line-frequency transformers for the purpose of enhancing their voltage or current rating. The use of line-frequency transformers, however, not only makes the converter heavy and bulky, but also induces the so-called dc magnetic flux deviation when a single-line-to-ground fault occurs [2].

The characteristics of the modular multilevel converter is low switching losses due to a considerably lower switching frequency ($f_s \approx 3f_l$), compared to a 2-level equivalent. Apart from the lower switching frequency, the quality of the output voltage waveform is higher. Thus smaller and simpler harmonic filters are required. A short circuit at the DC-bus will not discharge the storage capacitors therefore fault recovery is very fast [2]. The modular multilevel converter provides simplicity of design and control, as well as scalability to

various voltage and or power levels. Moreover, modular multilevel converter has the potential to improve the reliability, as a faulty module can be bypassed without significantly affecting the operation of the whole circuit.

The Modular Multilevel inverter is classified as Single Star Bridge Cells (SSBC), Single Delta Bridge Cells (SDBC), Double Star Chopper Cells (DSCC) and Double Star Bridge Cells (DSBC) [3]. The double-star-configured MMC topology possesses the common dc-link terminals as shown in Fig. 1, which enables dc-to-ac and ac-to-dc power conversion. However, the star/delta-configured MMC topology has no common dc-link terminals. As a result, it has no capability of achieving dc-to-ac and ac-to-dc power conversion although it can control active power back and forth between the three phase ac terminals and the floating dc capacitors [4]. This means that the star/delta-configured MMC topology is not applicable to industrial motor drives, but it is suitable for STATCOMs and energy storage systems. Compared to SSBC, SDBC, DSBC configurations, DSCC is superior and widely used because number of switches used in sub-module is half of bridge cell thereby switching losses reduces

and efficiency of the converter increases. Also DSCC does not require grid inductor and it is connected to grid directly [5]-[8].

II. STRUCTURE OF MODULAR MULTILEVEL INVERTER

The Fig. 1, shows the single phase equivalent circuit of five-level MMCI with Double Star Chopper Cell configuration [9]. The converter has one leg comprises of two arms including the upper arm and the lower arm, with each arm having four Sub-Modules (SM) and two non-coupled buffer inductors and an equivalent resistor. Each sub module comprises of two switches and one sub module capacitor as shown in Fig.2, which controls the output voltage of a module to be zero or capacitor voltage. The two non-coupled buffer inductors are inserted into the arms, since they do not disturb operation or generate overvoltage for the semiconductors [10], [11]. The buffer inductor can limit the AC-current [12], whenever the DC-Bus is short circuited (fault condition) and it act as passive filter during normal condition [13]. The DC Link of MMC is connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arm which is connected to

RL load and Fig. 1, produces N+1 level PWM waveforms by connecting N sub-modules constantly to the phase leg over entire fundamental period.

The level of voltage waveform is defined by the number of sub-modules connected to upper arm of the topology (N_{upper}) and are given by

$$\text{Level, } m = \frac{N}{2} - N_{upper} \quad (1)$$

The number of SMs in the lower arm of the converter (N_{lower}) is then

$$N_{lower} = N - N_{upper} \quad (2)$$

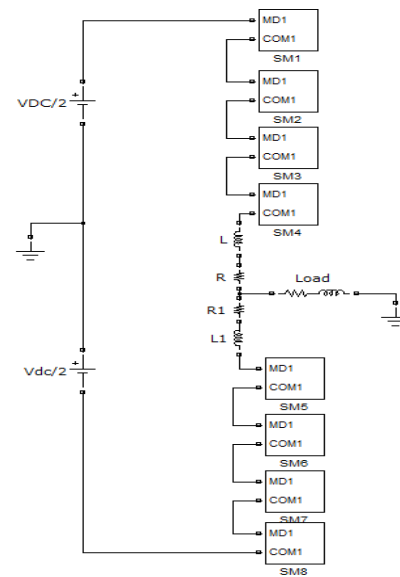
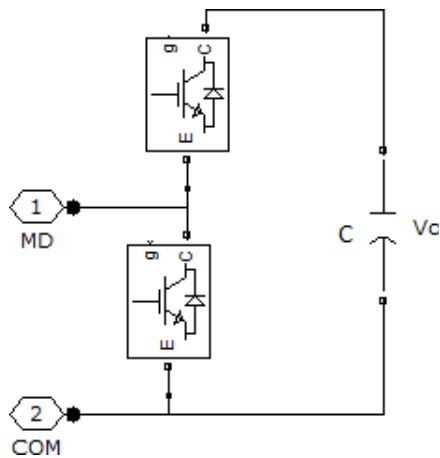


Fig. 1 Equivalent circuit of single phase five-level modular multi-level cascaded inverter.



**Fig. 2 Bidirectional PWM chopper-cell
with a floating dc capacitor**

III. CARRIER PHASE SHIFTED SINUSOIDAL PULSE WIDTH MODULATION

The capacitor voltage balancing control is based on CPS-SPWM. The CPS-SPWM is

the most commonly used modulation strategy for multilevel converter [14]. When CPS-SPWM is applied, the carrier of each module uses determinate frequency, but is phase-shifted. The determinate switching frequency offers convenience to balance the energy in each module and estimate the power loss for real industrial applications [15]-[19].

Compared with other modulation strategies, CPS-SPWM has certain advantages in balancing the capacitor voltage. In addition, the CPS-SPWM can reduce the generated harmonic voltages effectively using low switching frequency.

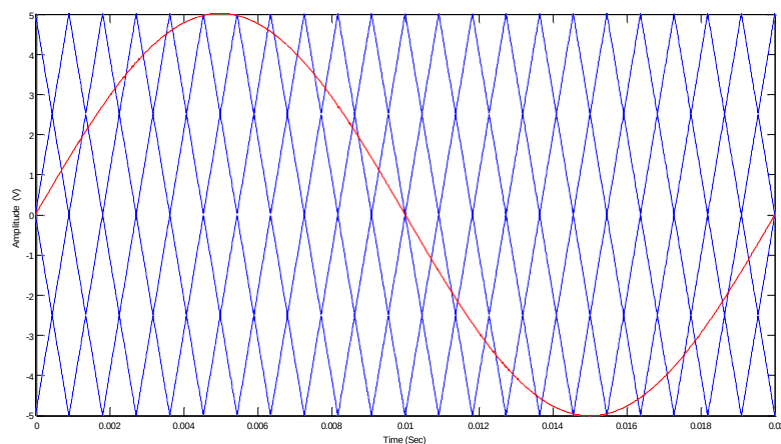


Fig. 3 Carrier arrangement for PSPWM strategy ($m_a=1$ and $m_f=23$)

The principle of CPS-SPWM suitable for MMCI is shown in Fig. 3. For a leg which consists of n sub-modules per phase, these n sub-modules use n triangular carriers whose phase is shifted by $2\pi/n$ from each other. It has to be emphasized that, from those n triangular signals, half of them belong to the phase upper arm sub-modules while the rest belong to the lower one. (Obviously, there is a phase difference of $(2 \cdot 360^\circ) / n$ between two consecutive triangular signals which belong to the same arm. The angular displacement θ_k can be expressed as

$$\theta_{kl} = \frac{2\pi}{N} k + \alpha \quad (3)$$

$$\theta_{ku} = \theta_{kl} + \beta \quad (4)$$

where α and β are arbitrary angular offsets which do not depend on the variable k . The angle α indicates the angular displacement between the reference waveform and the carrier waveforms, and the angle β indicates the angular displacement between the carrier waveforms in the upper and lower arms. In order to minimize the harmonic distortion in the direct voltage, the displacement of the carrier waveforms should be chosen such

that the switching harmonics are canceled out. This can be done by displacing the carrier waveforms in the upper arm by π radians from the carrier waveforms in the lower arm which gives that

$$\beta = \pi \quad (5)$$

This is referred to $(N+1)$ level modulation since this is the number of voltage levels that can be obtained at the ac terminal.

IV. VOLTAGE BALANCING CONTROL METHOD OF THE MODULAR MULTILEVEL CASCADED INVERTER

The capacitor voltage balancing control is based on CPS-SPWM and consists of averaging control and individual-balancing control [20]-[26]. Fig. 4 shows the principle of averaging control which forces the phase-R average voltage v_{Cr} to follow capacitor voltage reference v_C^* . Consequently energy is distributed into each module averagely. The phase-R average voltage v_{Cr} can be obtained by

$$V_{Cr} = \frac{1}{8} \sum_{j=1}^8 V_{Cjr} \quad (6)$$

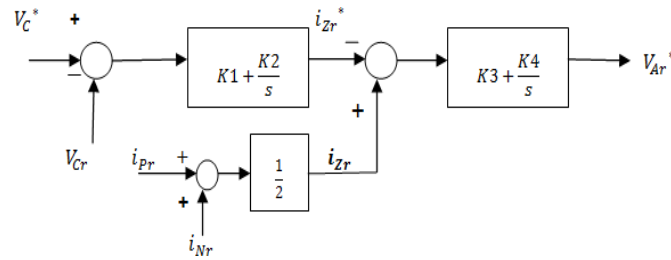


Fig. 4 Block diagram of DC-capacitor voltage control: Averaging control.

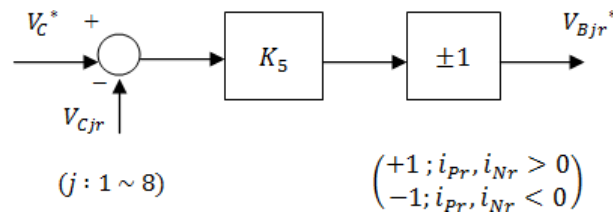


Fig. 5 Block diagram of DC-capacitor voltage control: Balancing control

As is shown in Fig. 4, averaging control includes two closed-loops. Both loops adopt proportional-integral control. The voltage loop enables the average voltage to follow its reference and the output is used as current reference of the current loop. The circulating current is adjusted in the current inner loop, and the dc-loop current reference of i_{zr} is i_{zr}^* , as shown in Fig. 4.

It is given by

$$i_{zr}^* = K1(V_C^* - V_{Cr}) + K2 \int (V_C^* - V_{Cr}) dt \quad (7)$$

The voltage command obtained from the averaging control,

V_{Ar}^* is given by

$$V_{Ar}^* = K3(i_{zr} - i_{zr}^*) + K4 \int (i_{zr} - i_{zr}^*) dt \quad (8)$$

The block diagram of individual-balancing control is shown in Fig. 5. The individual-balancing control forces the capacitor voltage of each module to follow its reference V_C^* . The difference of capacitor voltage and its reference is used as the input of a proportional controller, and then

multiplied by the arm current i_{Pr} (or i_{Nr}). The reference voltage for $j = 1 \sim 4$ from the balancing control is given by

$$V_{Bjr}^* = \begin{cases} K5(V_C^* - V_{Cjr}) & (i_{Pr} > 0) \\ -K5(V_C^* - V_{Cjr}) & (i_{Pr} < 0) \end{cases}$$

(9)

While V_{Bjr}^* for $j = 5 \sim 8$ is given by

$$V_{Bjr}^* = \begin{cases} K5(V_C^* - V_{Cjr}) & (i_{Nr} > 0) \\ -K5(V_C^* - V_{Cjr}) & (i_{Nr} < 0) \end{cases}$$

(10)

Fig. 6 and Fig. 7 shows a voltage command of each chopper-cell V_{jr}^* . The positive-arm and negative-arm commands are obtained as:

$$V_{jr}^* = V_{Ar}^* + V_{Bjr}^* - \frac{V_r^*}{4} + \frac{V_{dc}}{8} \quad (j : 1 \sim 4)$$

(11)

$$V_{jr}^* = V_{Ar}^* + V_{Bjr}^* + \frac{V_r^*}{4} + \frac{V_{dc}}{8} \quad (j : 5 \sim 8)$$

(12)

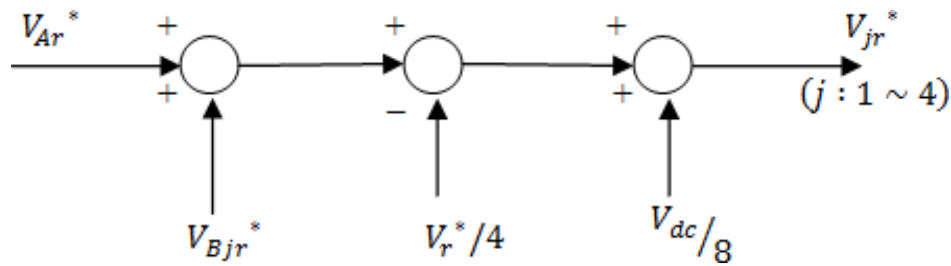


Fig. 6 Voltage command of Positive arm

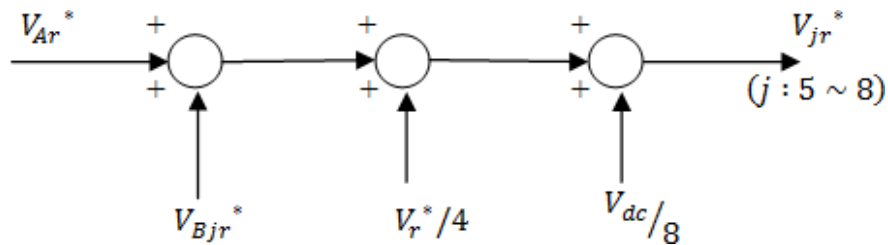


Fig. 7 Voltage command of Negative arm

Where V_r^* is an ac voltage command for the R-phase load. Fig. 4 includes the feed forward control of the dc supply voltage V_{dc} . The voltage command V_{jr}^* is normalized by each dc-capacitor voltage V_{Cjr} , followed by comparison with a triangular waveform.

V. SIMULATION RESULTS

To verify the validity of the proposed control strategy, the module shown in Fig. 1 for

single phase 5 - level modular multilevel cascaded inverter based on CPS PWM has been built using Matlab/Simulink and the simulated results are shown in the following sections.

Table 1 shows the parameters used for the simulation and Table 2 shows the control gains used for the simulation.

TABLE I Simulation Parameters

Parameters	Values
No. of sub-modules in each arm, N	4
No. of sub-modules per phase, n	8
Sub-module Capacitor, C	2.5 mF
Arm Inductor, L	1 mH
Arm Resistor, R	0.1
Carrier frequency per sub-module, fC	2.5 kHz
Converter switching frequency	10 kHz
Power frequency, f	50 Hz
Amplitude Modulation Index	0.9

Frequency Modulation Index	50
DC supply voltage	500 V
No. of voltage levels	N+1
Load	10 Ω , 10 mH

TABLE II Control Gains used for Simulation

Parameters	Variables	Values
Proportional gain of averaging control	K1	0.5 A/V
Integral gain of averaging control	K2	80 A/(V-s)
Proportional gain of current control	K3	1 V/A
Integral gain of current control	K4	640 V/(A-s)
Proportional gain of balancing control	K5	0.5

The load phase voltage, load current, upper arm current, lower arm current, both upper and lower arm current, capacitor voltage in upper arm, lower arm and average capacitor voltage in both upper and lower arm for RL load of single- phase five-level modular multilevel cascaded inverter employing CPSPWM is shown in Figs. 8 and 15.

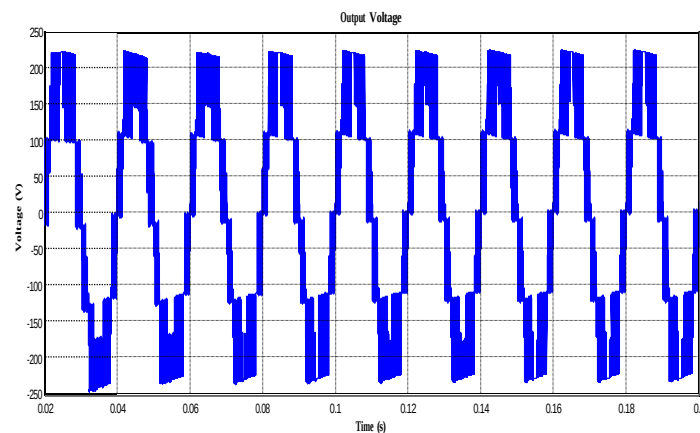


Fig. 8 Load Phase Voltage for RL load

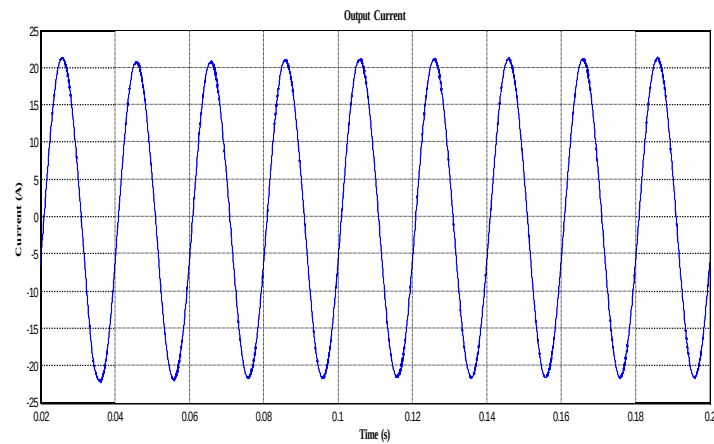


Fig. 9. Load current for RL load

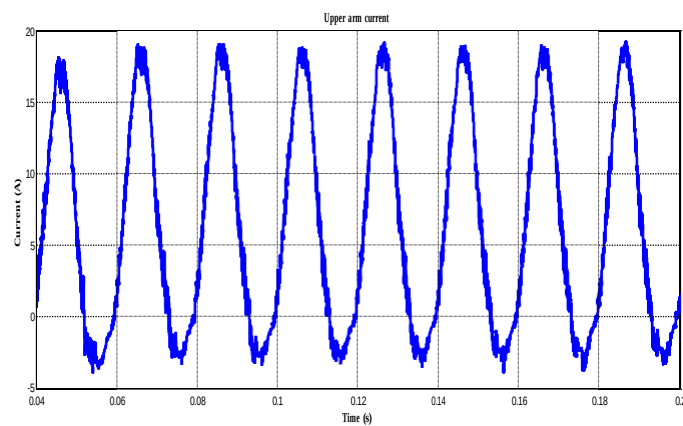


Fig. 10. Upper arm current for RL load

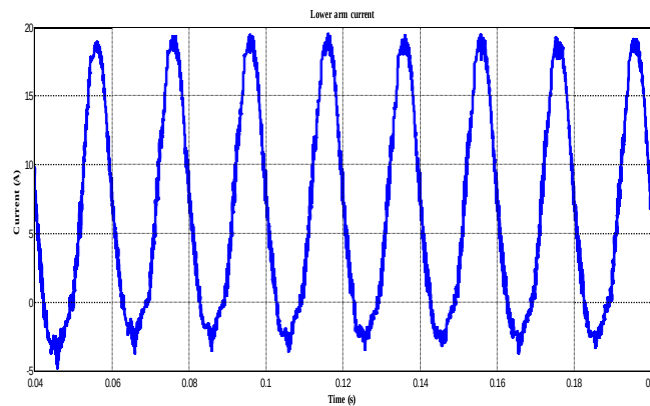


Fig. 11. Lower arm current for RL load

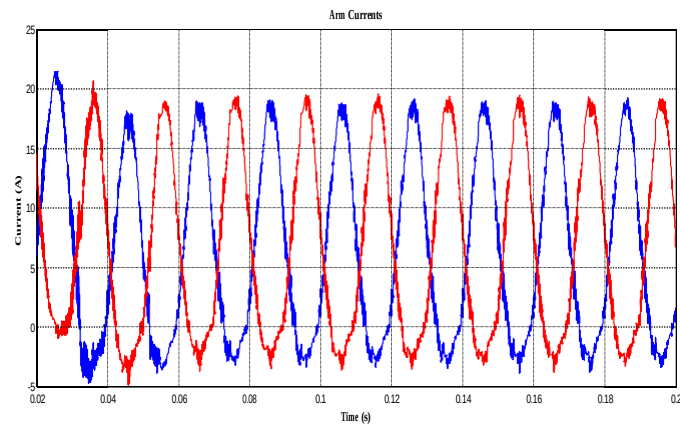


Fig. 12. Upper and lower arm currents for RL load.

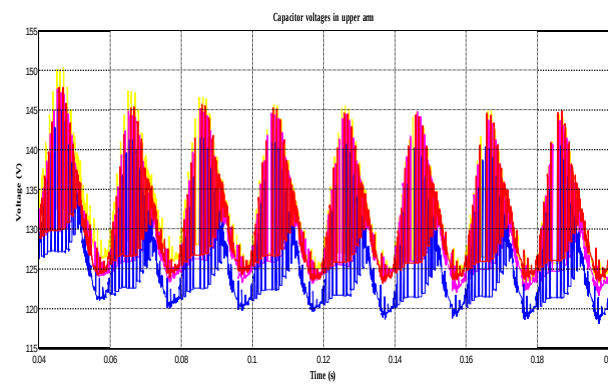


Fig. 13. Capacitor voltages in upper arm for RL load.

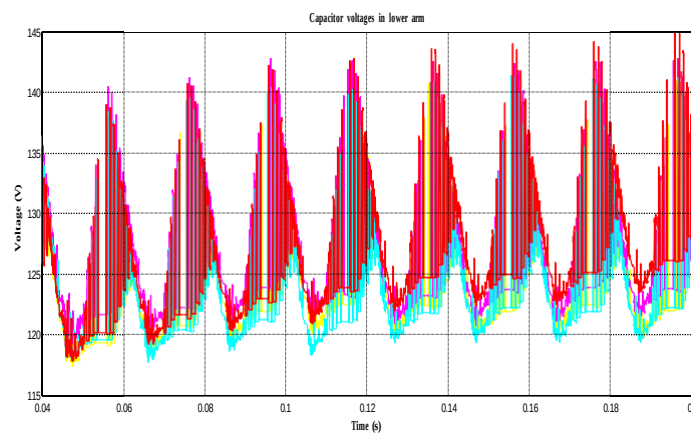


Fig. 14. Capacitor voltages in lower arm for RL load.

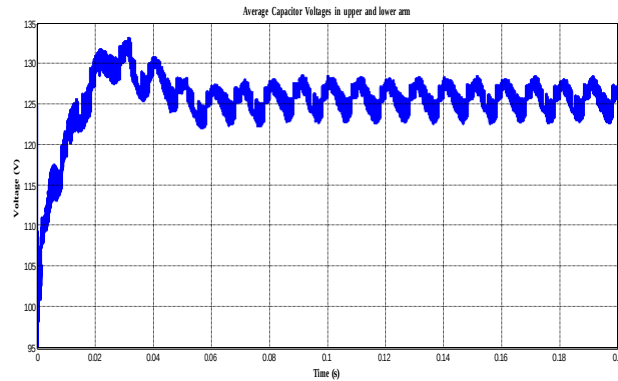


Fig. 15. Average capacitor voltages in upper and lower arm for RL load.

The harmonic analysis for phase voltage and load current with RL load is done using Fast Fourier Transform (FFT) as shown in the Figs. 16 and 17. The THD values obtained for phase voltage is 24.59% and load current is 1.44%.

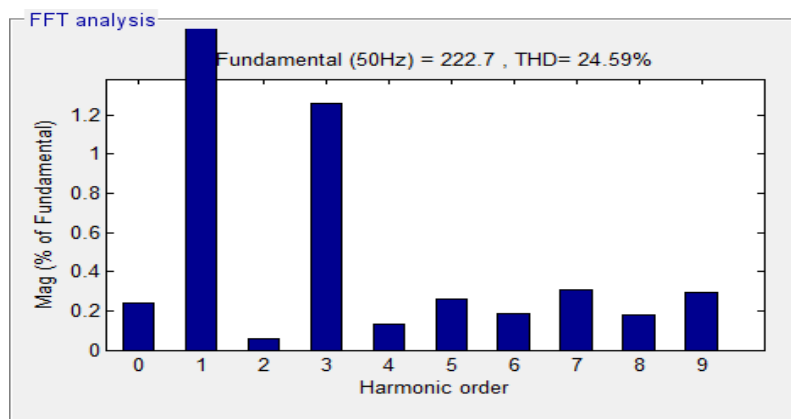


Fig. 16. Harmonic of the output phase voltage for RL load.

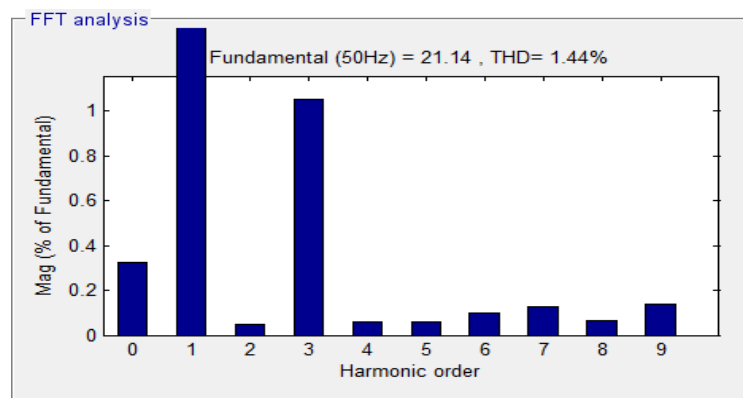


Fig. 17. Harmonic of the output current for RL load

CONCLUSIONS

In this paper, single phase five-level modular multilevel cascaded inverter based on double star chopper cells configuration employing CPSPWM multicarrier PWM strategies with RL load is simulated using Matlab/Simulink software. The averaging control and balancing control is implemented for voltage balancing of the sub-module capacitors and the effectiveness of the voltage-balancing control is validated based on simulation results. The THD of phase voltage is 24.59% and that of load current is 1.44% for the modulation index of 0.9. Thus, CPSPWM based capacitor voltage balancing control strategy for MMCI is the preferred control strategy producing a load voltage and output current with the least distortion.

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