

Reducing the Harmonic Using Dead Time Elimination Scheme for Inverter

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Abstract

In order to prevent the power switching devices (e.g., the Insulated-Gate-Bipolar-Transistor, IGBT) from shooting through in voltage source converter during a switching period, a dead- time is inserted in between the off going and turning on devices, either in the hardware drivers of the IGBTs or implemented in the software Sinusoidal Pulse-Width Modulation (SPWM) scheme. Both methods will lead to a degradation of the injected current power quality. This paper will present a dead-time elimination scheme for a SPWM controlled inverter. In comparison to using expensive current sensor, this method determines precisely the load of current polarity by detecting the terminal voltage of the anti-parallel diode of power devices. The presented scheme includes the freewheeling current polarity detection circuit and the PWM control generator without dead-time. This method significantly reduces the output voltage loss and harmonic distortion, and improves quality of power. Simulation results are given to demonstrate the effectiveness of the dead-time elimination scheme.

Keywords: *Dead time, PWM, Sinusoidal Pulse Width Modulation (SPWM), Harmonics*

INTRODUCTION

Use of power electronic converters has made it increasingly more challenging to maintain power quality in the grid-

connected renewable energy systems like Photovoltaic (PV) and wind turbinesystems [1], [2], due to a) the intermittent nature of renewable energies [3] and b) Pulse-Width Modulation (PWM)

control of the power converters [3], [4]. In order to alleviate the harmonic injections from the grid-connected PWM converters, many advanced current controllers have been developed, like the Proportional Resonant (PR) controller [5]–[8]. With these controllers, the current quality can be improved to some extent in terms of a lower Total Harmonic Distortion (THD). Using higher-order passive filters (e.g., LCL filter) [9] is an alternative, as it contributes to a further enhancement of the power quality, however it leads to more power losses, increased complexity, and higher cost [10].

Increasing the switching frequency increases the possibility of using smaller output filters and thus, lowers the cost, but the non-linearity like the dead time effects will be magnified and thus, the current quality will be poorer [11]. Nevertheless, in practice, the dead time has to be implemented in the PWM drivers to prevent the inverter from shoot through during a switching interval [12]–[21]. However, it also introduces potentially harmonic problems in the PWM converters [13]–[15].

Most dead time compensation methods are based on an average value theory [12], [15], [16], [18]. In those techniques, the

voltage lost because of the dead time is averaged over an entire period, and the resultant value is correspondingly added to the inverter voltage reference in order to compensate for the dead time effect. However, these methods rely on the detection of the current polarity, leading to an increase of the overall complexity and also a decrease of noise immunity at zero crossing points of the current. Moreover, such methods cannot correctly estimate the lost voltage around zero current points as discussed in [18]. Thus, other dead time compensation solutions have been reported in the literature [16], [18], [22]–[24].

For instance, in [16], a compensation method using the controller integrator output has been introduced, and in [18], an adaptive dead time compensator has been developed, which calculates the feed-forward compensation duty cycle. In addition, since the dead time mainly introduces low order harmonics [16], it is possible to mitigate these harmonics simply by using multiple ReSonant Controllers (RSCs). This technique can effectively compensate the low order harmonics, but may also trigger the system resonance when higher order harmonics (e.g. 11th- and/or 13th-order harmonics) are compensated in order to fully mitigate

the dead time effect.

In contrast, a Repetitive Controller (RC) based on the internal model principle [25]

can suppress all the harmonics (including the harmonics induced by the dead time) without the concern of resonance if it is designed properly, and this might be a promising solution for the harmonic compensation. Therefore, this paper presents harmonics mitigation method for the dead time effects based on an RC in § III after a brief introduction of the control of single-phase grid-connected inverters. The RC based solution for the dead time compensation does not require additional hardware modifications as well as complicated mathematical derivations. When it is implemented in a digital controller, the RC is plugged in parallel with a PR fundamental-frequency controller as the harmonic compensator. In order to verify the effectiveness of the RC based dead time harmonic mitigation, experiments have been performed on a 2-kW single-phase grid-connected inverter system, and the testing results are provided in § IV.

In addition, comparisons between the RC based mitigation method and the RSC based dead time compensation solution in

the case of grid voltage background distortions are also carried out before the conclusion. EFFECT OF DEAD TIME

When AC induction motors are operated using open-loop adjustable frequency drives, system instabilities may occur for certain frequency ranges and loading conditions. The cause of these instabilities can be inherent low-frequency motor instabilities, instability due to the interaction between the motor and the PWM inverter, or the choice of PWM strategy.

When the AC induction motor is fed by the voltage source inverter, the applied stator voltage waveforms contain harmonics generated by the PWM algorithm. The system stability will be affected by these harmonics, especially at low frequencies and no load conditions, causing additional machine losses and reduced efficiency. The magnitude of these losses will depend on the magnitude of the harmonic content in the applied voltage and are compounded by induced harmonics. Excessive harmonics will increase motor heating and torque pulsations. Even the smallest of harmonics as a percent of the fundamental, when coupled with the motor, can result in unstable operation. The choice of the PWM strategy is then important to

minimize the voltage and current harmonics. Defects in the PWM strategy will result in voltage deviations at the motor terminals and will be intensified by the addition of the inverter dead time.

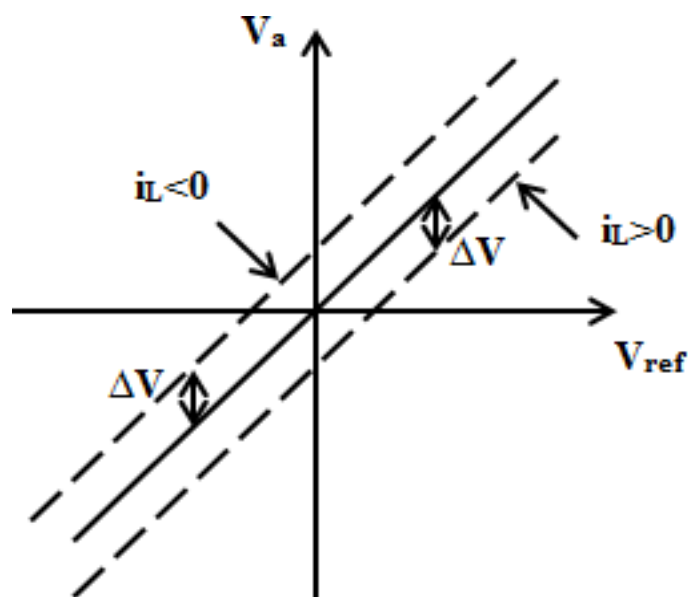


Fig-1 Dead time effect

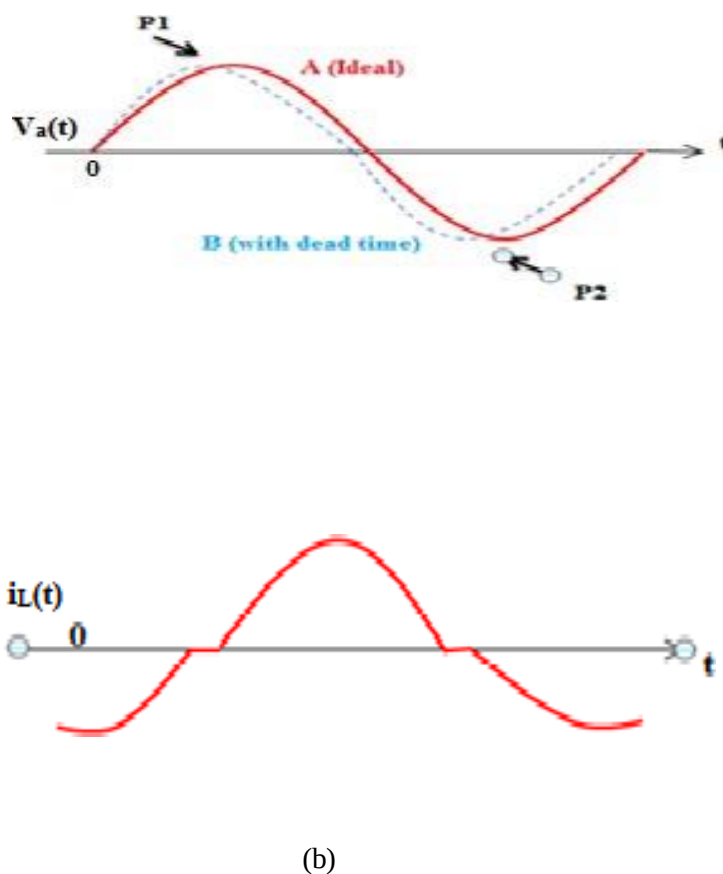
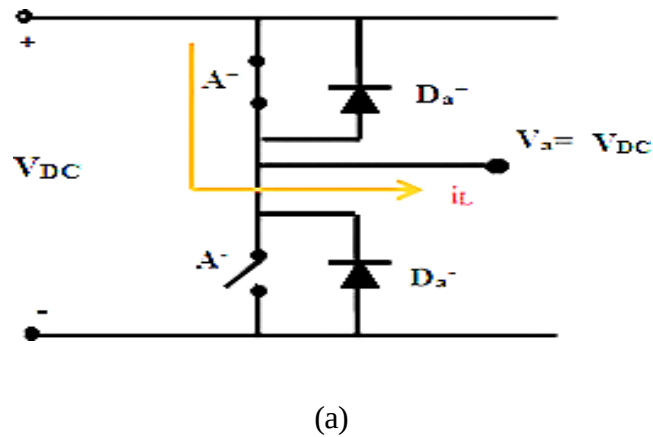


Fig-2 Voltage distortion caused by dead time (a) Inverter/converter leg. (b) Voltage distortion caused by dead time

The effects of the dead time on the output voltage are shown in Fig. 1. It can be examined from one phase of the PWM inverter. The basic configuration shown in Fig. 2 consists of upper and lower power devices A^+ and A^- , and reverse recovery diodes Da^+ and Da^- , connected between the positive and negative rails of the power supply.

Commutation of the power devices comes from the PWM generator. Output terminal V_a is connected to motor phase V_a and the current i_L is positive with respect to the motor. Examining the power device switching sequence as A^+ is turning OFF and A^- turning ON, or A^- is turning OFF and A^+ turning ON, there exists a time when both power devices cease to conduct. During the dead time output V_a appears to be floating, but the current i_L must conduct through reverse recovery diodes Da^+ and Da^- . Depending on the current polarity, the reference voltage may be delayed by the dead time.

Consider the four possible commutation sequences.

In the first condition, the current i_L is positive. A^+ transitions from ON to OFF and A^- from OFF to ON. During the dead zone, Da^- conducts and Da^+ blocks

the flow of current to the positive rail. This condition results in the correct voltage applied to the motor terminals.

In the second condition, the current i_L is positive. A^+ transitions from OFF to ON and A^- from ON to OFF. During the dead zone, Da^- continues conduction and Da^+ blocks the flow of current to the positive rail. Current conducts in $D2$ until the dead time elapses, then A^+ turns ON. This condition results in a loss of voltage at the motor terminals.

In the third condition, the current i_u is negative. A^+ transitions from OFF to ON and A^- from ON to OFF. During the dead zone, Da^+ conducts and Da^- blocks the current flow to the negative rail. This condition results in the correct voltage applied to the motor terminals.

For the fourth condition, the current i_L is negative. A^+ transitions from ON to OFF and A^- from OFF to ON. During the dead zone, Da^+ continues conduction and Da^- blocks the flow of current to the negative rail. Current conducts in $D1$ until the dead time elapses, then A^- turns ON. This condition results in a gain of voltage at the motor terminals.

Fig. 3 shows the effect of dead-Time. Trace 3a and 3b are the ideal pulse times;

if applied, the resulting fundamental voltage would be of the correct magnitude and phase.

In trace 3c, A⁺ transitions from ON to

OFF, but there must be a delay time before A⁻ in trace d can turn from OFF to ON. Likewise as A⁻ in trace 3d transitions from ON to OFF, A⁺ in trace 3c must delay before it can turn on.

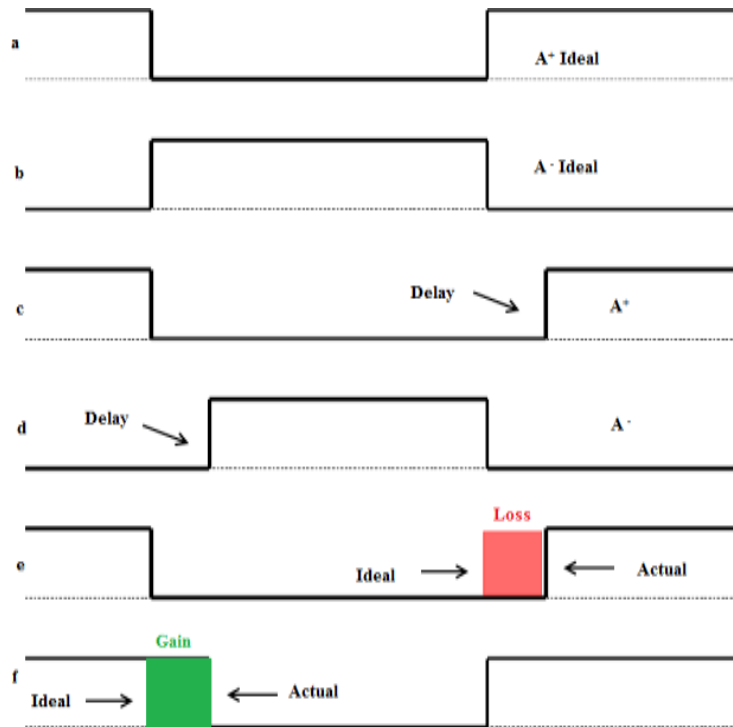


Fig-3 Pulse deviations (Afarulrazi and Zarafi, 2010)

Consider in positive in trace 3e, as $A+$ transitions from ON to OFF, there is no reduction or gain to the pulse time as compared to the ideal pulse time. As $A+$ transitions from OFF to ON, the pulse time decreases from the ideal resulting in a deviation to the pulse time and an incorrect fundamental voltage to the load.

When i_u is negative as in trace 3f, $A+$ is held on longer than the ideal, resulting in an increase in pulse time, and an incorrect fundamental voltage applied to the load. As $A+$ transition from OFF to ON, there is no reduction or gain to the pulse as compared to the ideal pulse

Therefore, the real output voltage is greater (smaller) than its command as current is negative (positive). Fig. 2 shows the phase voltage and current of the inverter output. As shown in Fig. 2, the output voltage $v_o(t)$ is with distortion as compared to that without dead time (see waveforms A and B). However, waveforms A and B cross each other at points P1 and P2. The output current $i_o(t)$ is also distorted at these two zero-crossing points, as shown in Fig. 2.

PROPOSED DEAD-TIME ELIMINATION SCHEME

a) PWM Generator without Dead Time

Fig. 3(a) shows the circuit of an inverter leg or half-bridge of converter. As shown in Fig. 3(a), an anti-parallel diode is connected with a power device. As the power device is off while the current conduction continues, the anti-parallel diode of its opposite power device provides the current path. Therefore, there is no need to turn on the opposite power device during this turn-off period. Once no switching occurs to its opposite power device, dead time is no more needed.

For example, when power device " $A+$ " is turned off and the current direction retains, " $Da-$ " will provide the current path when power device " $A+$ " is turned off. Similar facts occur to power device " $A-$ " and diode " $Da+$ ". Therefore, power device " $A+$ " and diode " $Da-$ " are defined as a " P " cell for positive current control (current flowing into the load side), as shown in Fig. 3(b). In addition, power device " $A-$ " and diode " $Da+$ " are defined as " N " cell [as shown in Fig. 3(b)], which conducts negative current.

Fig. 4 shows the PWM control without dead time. As shown in Fig. 4(a), once current is positive, P -cell control is retained. Meanwhile, there is no PWM

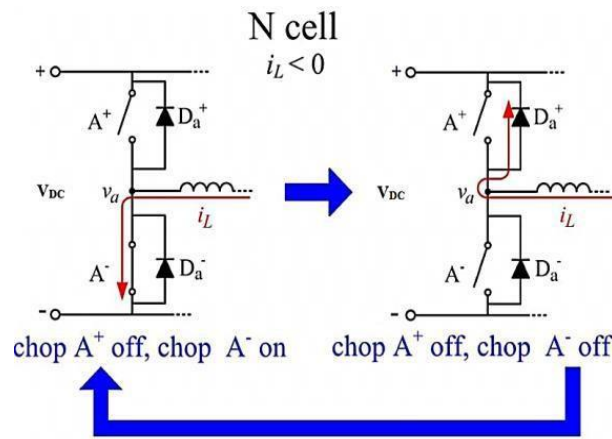
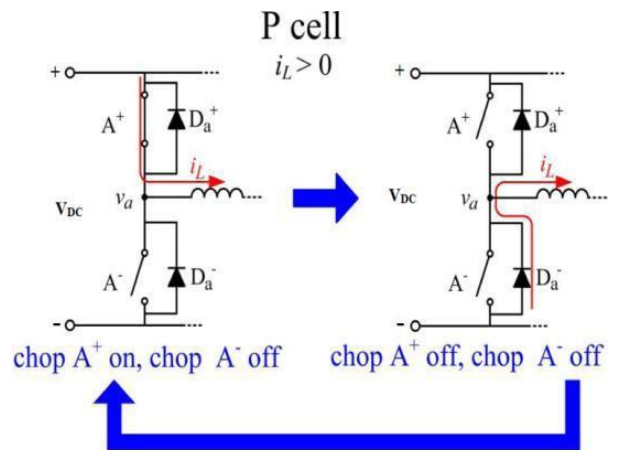


Fig-4. PWM control based upon P cell and N cell. (a) P-cell control, $i_L > 0$. (b) N-cell control, $i_L < 0$

control signal for N-cell control. Therefore, dead time is no longer required while guaranteeing no short through between positive and negative dc links. Similarly, when current is negative, a PWM control signal is applied to N cell only. Since there is no switching in the power device of P

cell, dead time is no longer needed, and no short through will occur.

Fig. 5 shows the relationship between the chop signals and the control signals of converter without dead time. The control signals can therefore be summarized as follows:

$$\text{Chop } A^+ = \text{chop} \cdot \text{sign}(i_L) \quad (1)$$

$$\text{Chop } A^- = \text{chop} \cdot \text{sign}(i_L) \quad (2)$$

As shown in (1) and (2), the required calculation is simple, and only slight modifications to the PWM signal are

required. Furthermore, the modifications can be realized by a digital controller. For inverter control, the chop signal is changed to a PWM control signal. The PWM generator can be realized using (1) and (2).

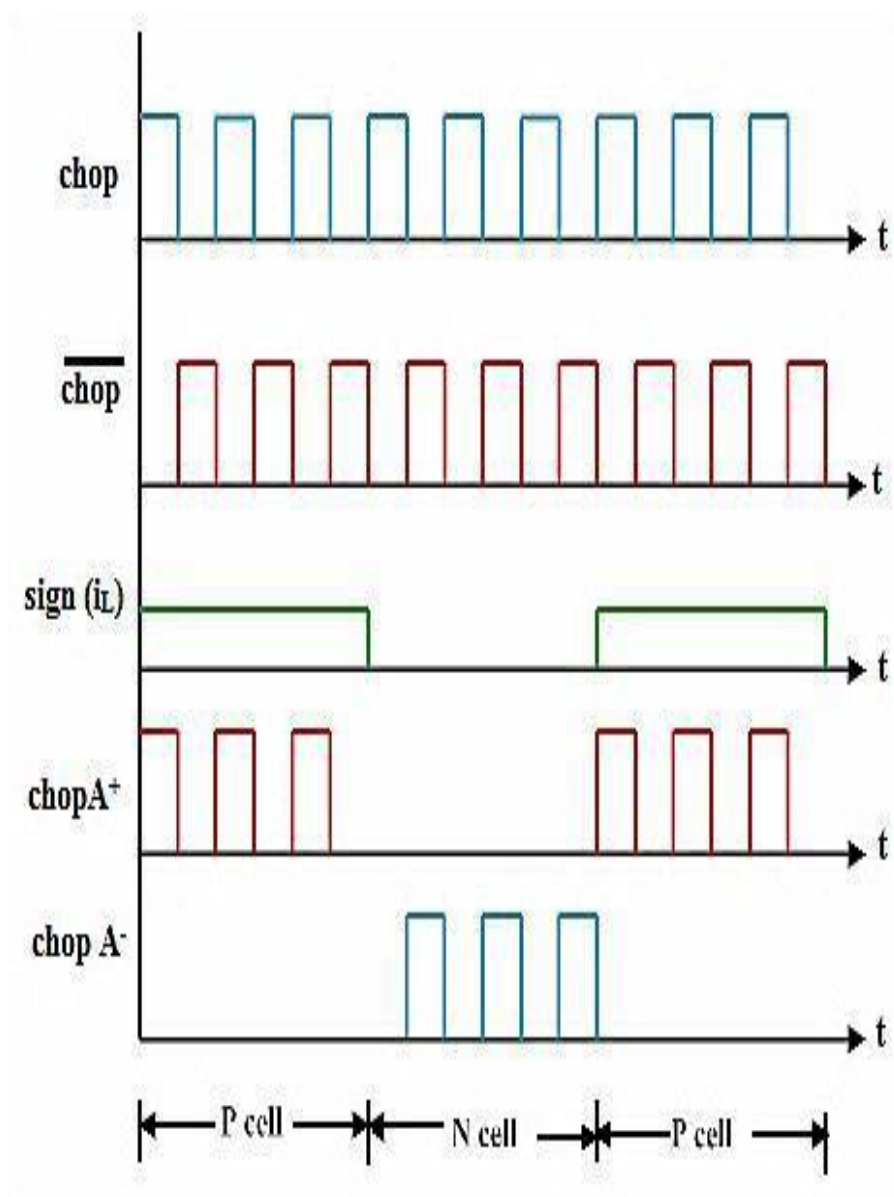


Fig-5 Signals for PWM generator

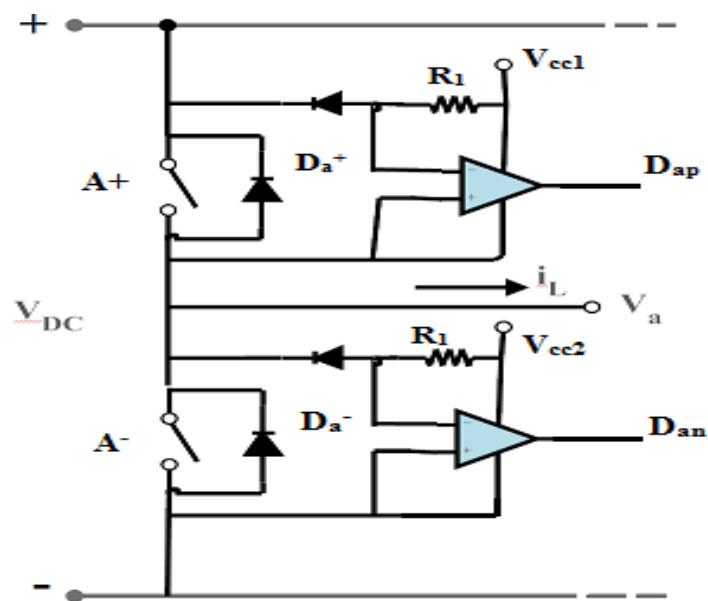


Fig-6. Previous detection circuit (Artur)

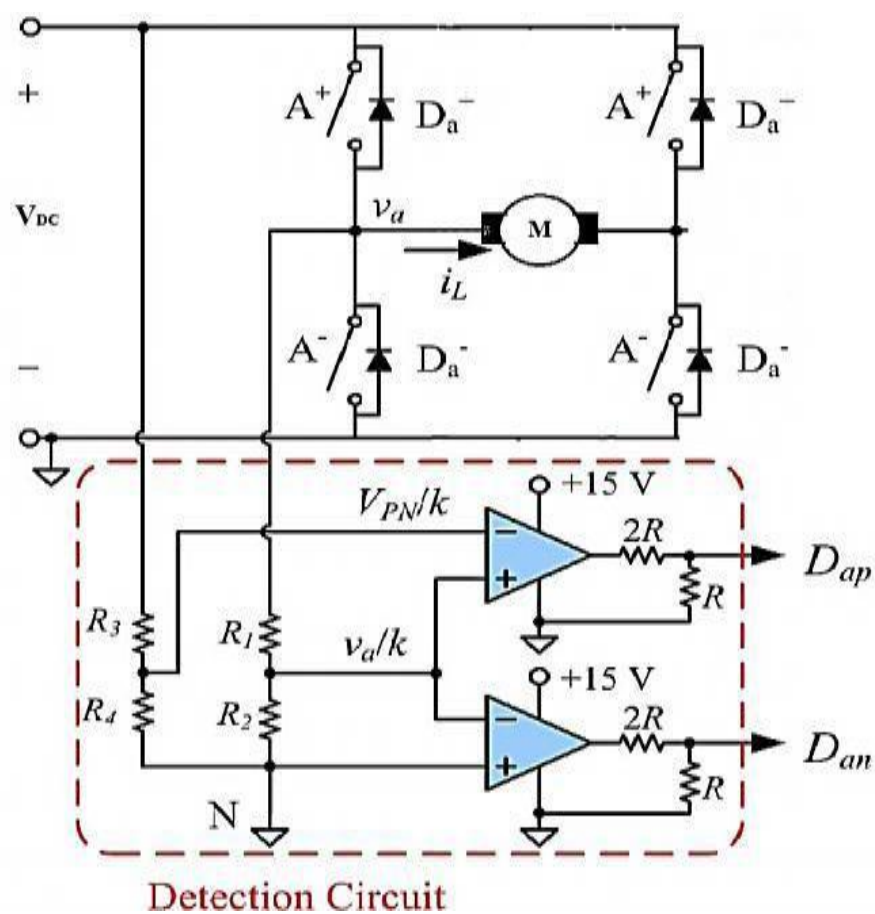


Fig-7. Proposed detection circuit

b) Freewheeling-Current Polarity Detection Circuit without Isolated Power

Fig. 6 shows the polarity detection of freewheeling current. The detection circuit requires two separate power sources, namely, “Vcc1” and “Vcc2,” as shown in Fig. 6. The required number of separate power sources is increased up to four for a three-phase inverter. These separate power sources increase the difficulty in modularization of the detection circuit.

Fig. 7 shows the presented freewheeling-current polarity detection circuit. As shown in Fig. 7, only one power source is required for the detection circuit for both single- and multiphase inverter/converter. This special feature enables the potential for modularization of the detection circuit. In Fig. 7, when $i_L > 0$, the terminal voltage becomes negative during the switch-off period, as shown in Fig. 8(a). Similarly, during the switch-off period, the terminal voltage is positive and greater than the dc-link voltage when $i_L < 0$, as shown in Fig. 8(b). Therefore, the terminal voltage can be used to reflect the polarity of freewheeling current. Once the polarity of current is determined, the control signals of converter/inverter can be generated by (1) and (2).

c) Freewheeling-Current Polarity Detection for Current with Multiple Zero-Crossing Points

Under some conditions, e.g., small inductor of load, the output current polarity changes very quickly in the zero-crossing area. There may be a few zero-crossing points, as shown in Fig. 9.

To deal with such an ambiguous situation, the concept of average current is used as an assistance index for the judgment of current polarity. Note that no real average value of load current is calculated. Once the period between “chop off” and zero crossing point is slightly greater than $0.5(1 - D)t_s$, the average current becomes negative, and the current polarity is changed. The polarity change rule is therefore modified as follows. If

$$t_k > 1/2(1-D)t_s \quad (3)$$

Then $i_{L,avg} > 0$, and there is no change of current polarity. If

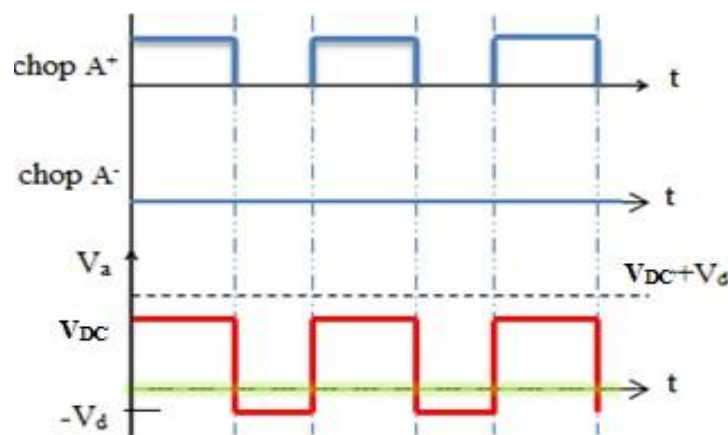
$$t_k \leq 1/2(1-D)t_s \quad (4)$$

Then $i_{L,avg} \leq 0$, and the current polarity is changed,

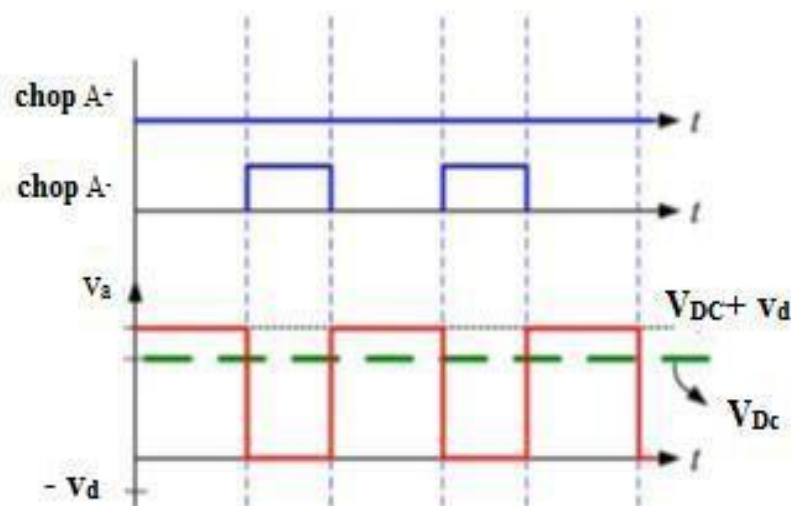
Where t_k = time interval between “chop off” and zero-crossing point ($k = 1, 2, 3$).

The presented circuit for the dead-time elimination circuit and the method are very effective. In the presented paper,

dead time is not required, and the power device (e.g., high-side power device) is turned on only when the antiparallel diode of its counterpart (low-side power device) is conducting current. Therefore, the possibility for ZVS seems dim.



(a)



(b)

Fig-8. Terminal voltage and PWM control signals without dead time. (a) $i_L > 0$ (b) $i_L < 0$

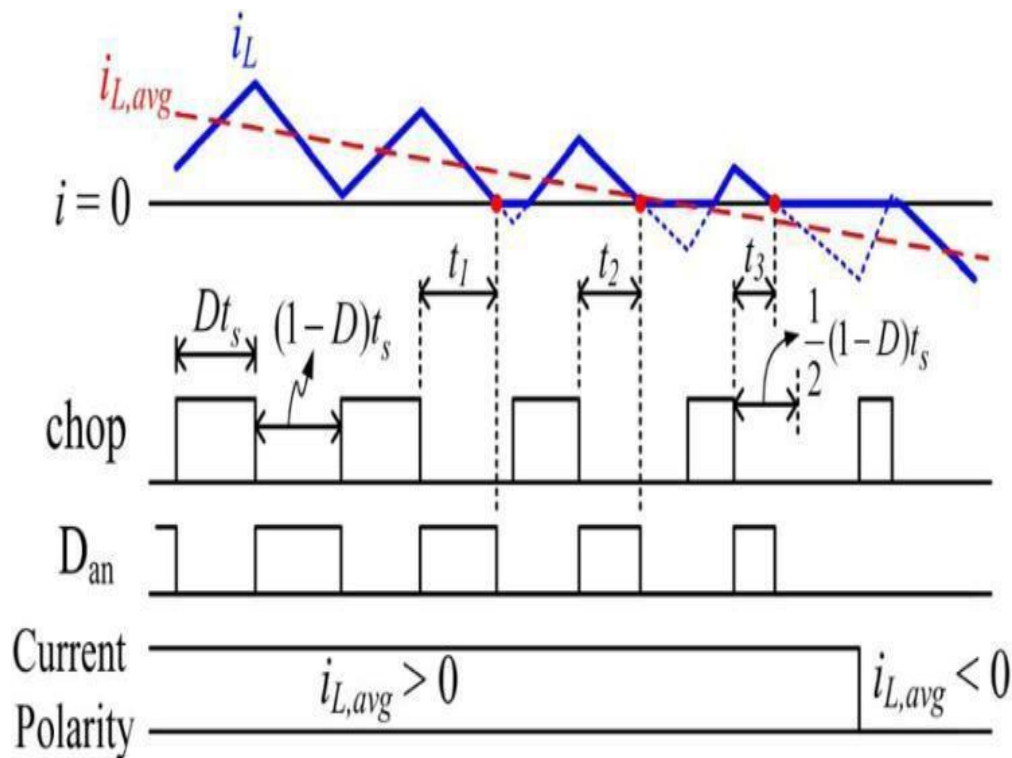


Fig-9 Load current with several crossing points around zero-current area

SIMULATION RESULTS

Fig. 10 shows the flowchart of the PWM generator without dead time. The “P”-cell control signal is switched on and off when current is negative. The polarity of freewheeling current is detected regularly with a sampling frequency which is higher than the switching frequency to reduce the detection error. In this section, the simulation performed by MATLAB software is carried out to verify the proposed method. The schematic of the SPWM voltage source converter power stage used for the simulation is shown in

Fig.11. the induction motor is chosen for the load of the inverter.

The simulations with both the conventional SPWM strategy with dead time and the proposed method are carried out for comparison. Fig. 4 shows the simulation waveform of i_L using the conventional PWM strategy with dead time. From the simulation results it can be seen that the output current is distorted. Fig. 12(b) shows the simulation waveforms using the proposed Method. From Fig. 12(b) it can be seen that the switch commands to the upper and lower

device of phase A, A+ and A- are complementary and without dead time.

As shown in Fig. 11, the proposed method can detect the polarity, and the PWM control signals do not require any dead

time. Since the dead time for the presented method is eliminated, the current distortion associated with dead time can be removed.

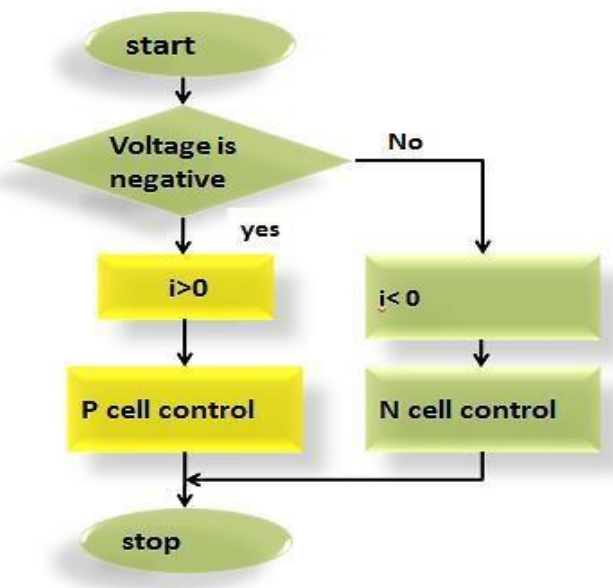


Fig-10 Flowchart of implementation

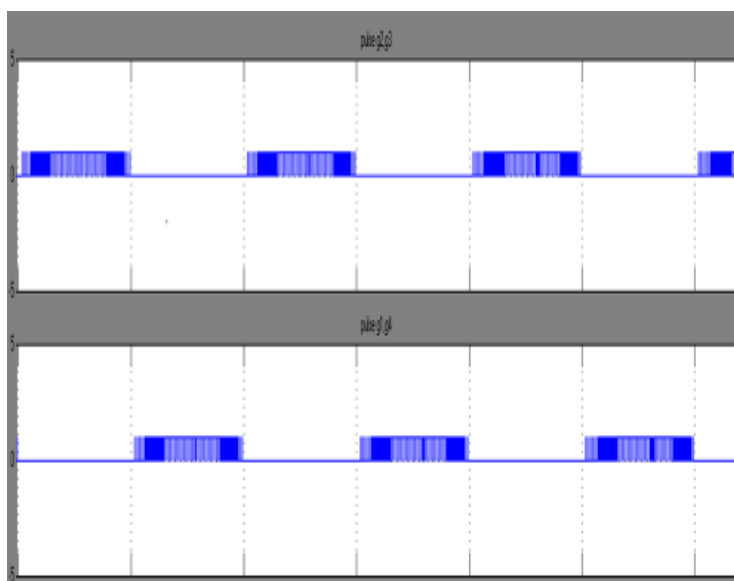
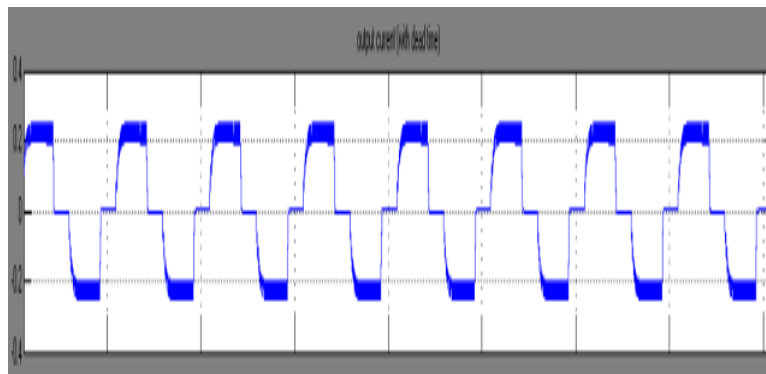
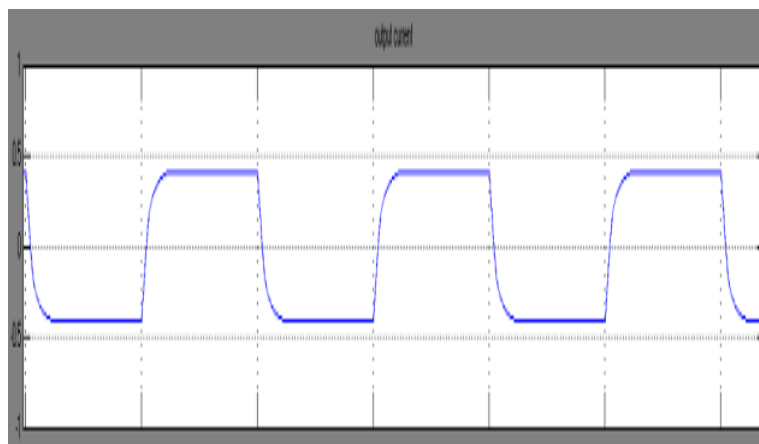


Fig-11 Gate pulses without dead-time



(a)



(b)

Fig-12 Current waveforms (a) With dead-time (b) Without dead-time

THD ANALYSIS SPWM is an effective technique used for variable frequency drive applications. It utilizes DC bus voltage more effectively and generates less THD in the Voltage Source Inverter.

SPWM utilize a switching frequency to spread the harmonics continuously to a wide band area so that the peak harmonics can be reduced greatly. Simulation has

been carried out by varying the modulation index between 0 and 1. Finally, performance of SPWM has been compared with and without dead time. The harmonic spectrum of SPWM inverter with and without dead time is shown in fig. 14.

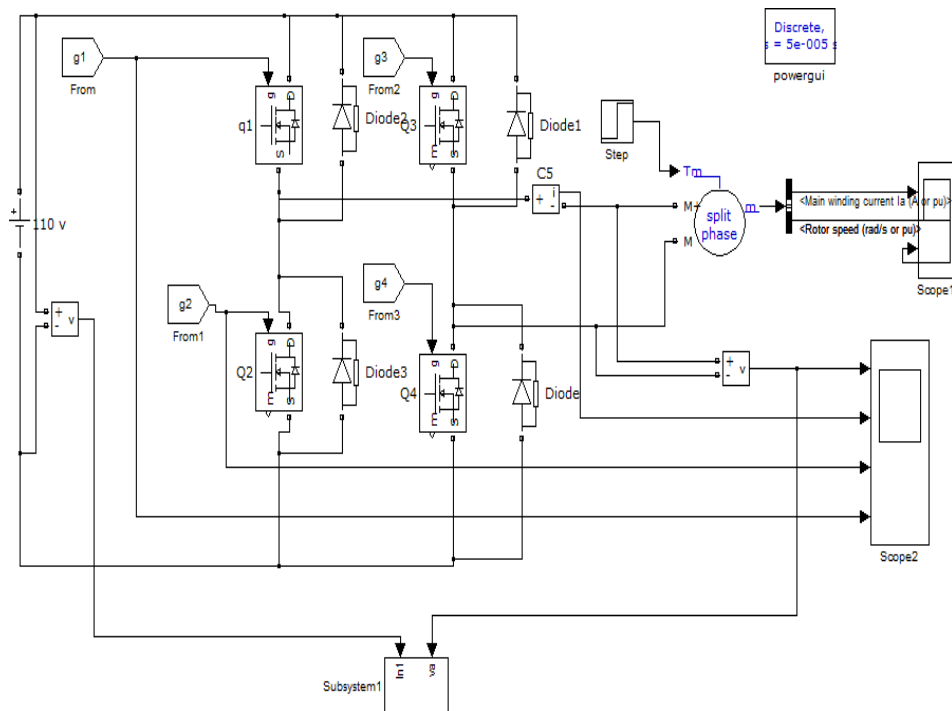
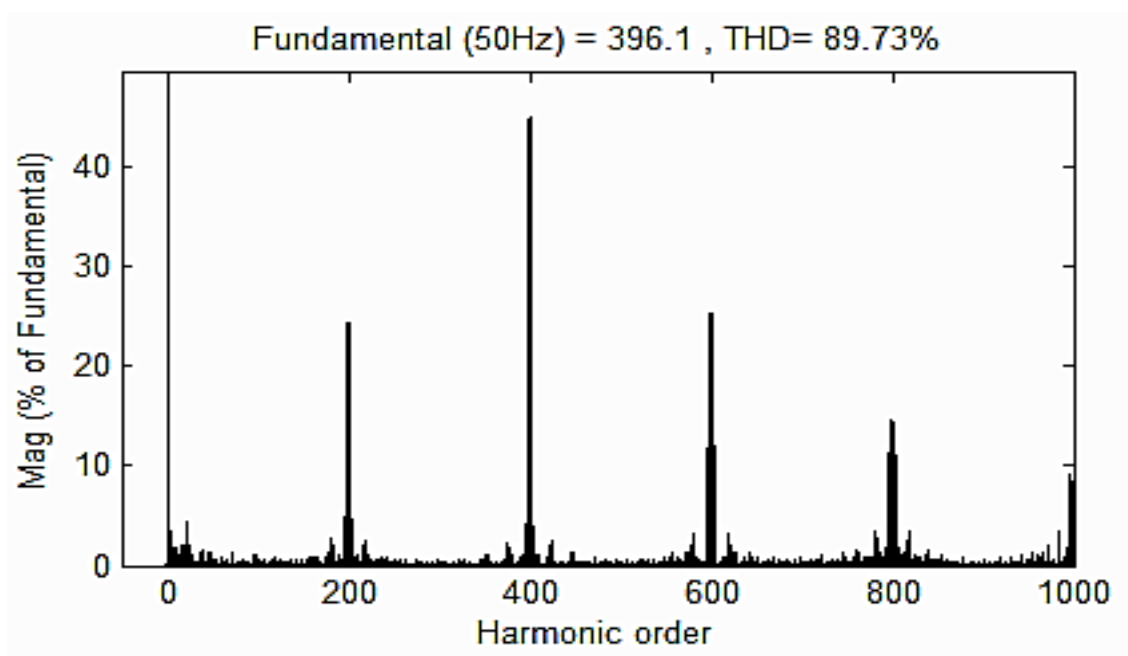
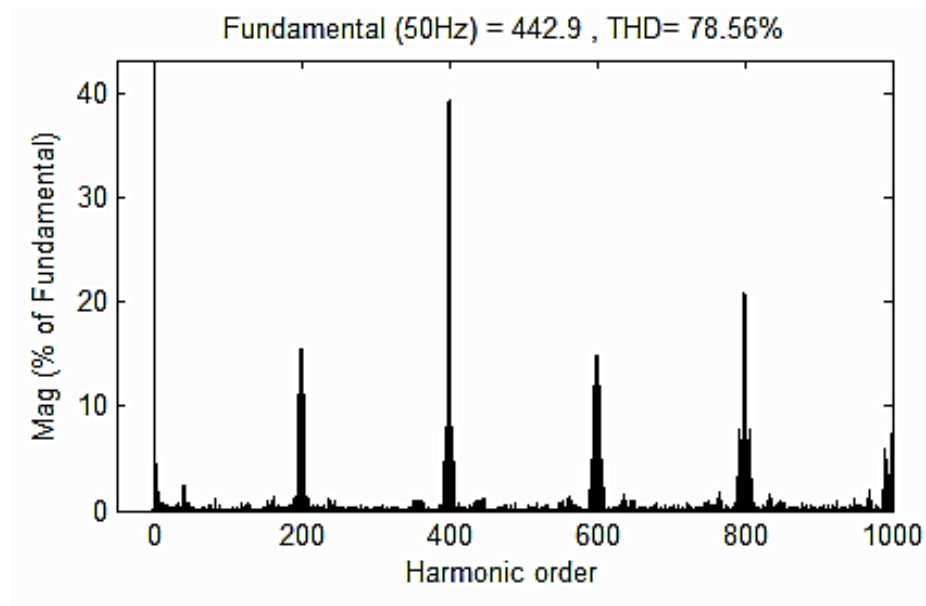


Fig-13 Simulation Diagram



(a) THD with Dead-Time



(b) THD without Dead-Time

Fig-14 Harmonic spectrum of SPWM inverter

CONCLUSION

In this paper, a method is proposed to eliminate dead time in the SPWM controlled inverters. Compared to the conventional method that involves dead-time, this method significantly reduces the output distortion and THD and improves the performance of the load. The main objectives of this paper include the following:

1. To propose a current polarity detection circuit that requires only a single power source for inverter.
2. Present the PWM control method without dead time based upon the

proposed current polarity detection circuit

3. To showcase that flexible implementation makes it an attractive option for VSI applications.

This method can be used in the voltage source PWM converter to enhance the performance, improve the reliability, and reduce the cost.

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