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Timing & Power Integrity Analysis in Sub-nm Designs

***Dharmendra Ray*[1]*, Balram Pathak*[2]*, Surabhi Chauhan*[3]*, Baban Tiwari*[4]**
***Associate Professor*[1]*, Assistant Professor*[2]**
Department of Heterogeneous Multi-Core Chip Design
Vidya Institute of Technology, India
Email: *Dharmendrarayi44@gmail.com*[1]*, balrampathak95r@rediffmail.com*[2]*, Surabhichauha1n@yahoo.com*[3]

Abstract

As semiconductor technology approaches the sub-nanometer (sub-nm) regime, ensuring reliable operation of integrated circuits (ICs) becomes increasingly challenging. Both timing and power integrity critically influence performance, yield, and reliability in advanced technology nodes. Sub-nm designs face heightened variability, increased leakage currents, and significant signal and power noise, making traditional analysis methods insufficient. This paper reviews state-of-the-art techniques in ***timing and power integrity analysis****, highlighting challenges specific to sub-nm designs, methodologies for mitigation, and emerging trends in modeling, simulation, and validation. Furthermore, the paper discusses multi-objective approaches that balance power, performance, and area (PPA) while maintaining signal and power integrity. Finally, case studies, tools, and methodologies are examined to guide designers in practical sub-nm IC design workflows.*

Keywords: *Sub-nm VLSI, Timing Analysis, Power Integrity, Signal Integrity, EM/IR Analysis, Variation-Aware Design, Advanced Nodes.*

INTRODUCTION

Scaling CMOS technology into the sub-nm regime (e.g., 3 nm, 2 nm, and below) has brought unprecedented challenges to IC design. While transistor density continues to increase, maintaining

timing and power integrity becomes a complex interplay of process variation, parasitics, thermal effects, and electromigration.

Timing integrity ensures that signals propagate through logic and interconnects without violating setup and hold constraints. Violations lead to functional errors and reduced yield. Meanwhile, **power integrity** focuses on delivering stable voltage levels across the chip while minimizing IR drop and noise, which can adversely impact both timing and reliability.

In sub-nm nodes, the interplay between **high-performance requirements** and **power constraints** requires designers to adopt holistic methodologies that combine modeling, simulation, and optimization techniques.

Challenges in Sub-nm Designs

Sub-nm designs encounter multiple critical challenges:

Increased Variability

- **Process Variations:** Random dopant fluctuations, line-edge roughness, and gate length variability significantly affect transistor characteristics.
- **Environmental Variations:** Temperature gradients and voltage fluctuations impact both timing and leakage currents.
- **2.2 Signal and Interconnect Limitations**
- **RC Delay Dominance:** As feature sizes shrink, interconnect resistance and capacitance dominate timing delays.
- **Crosstalk:** Neighboring interconnects introduce coupling noise, affecting timing margins.
- **2.3 Power Delivery Network Challenges**
- **IR Drop:** Voltage drops across metal layers affect circuit speed and reliability.
- **EM (Electromigration):** High current densities in sub-nm metal lines increase EM susceptibility.

Leakage and Dynamic Power

- **Subthreshold Leakage:** Increasingly significant in ultra-thin gate oxides.

- **Dynamic Power Spikes:** Rapid switching events can lead to transient voltage drops affecting timing margins.

Timing Analysis Techniques

Timing analysis ensures that signals propagate through digital circuits within prescribed time limits, avoiding setup and hold violations. In sub-nm designs, shrinking transistor sizes, increased interconnect delays, and variability make timing analysis more challenging. The evolution of timing analysis has moved from simple worst-case static approaches to **dynamic and variation-aware methods**, capable of addressing process, voltage, temperature (PVT), and noise effects simultaneously.

Static Timing Analysis (STA)

Static Timing Analysis (STA) remains a foundational technique in modern IC design. Unlike dynamic simulation, STA does not simulate every possible input vector. Instead, it evaluates **timing constraints along all paths** in a netlist using delay models derived from libraries.

Key Steps in STA:

1. **Path Enumeration:** STA identifies all paths between sequential elements (flip-flops, latches).
2. **Delay Calculation:** Each gate and interconnect delay is estimated using technology libraries.
3. **Setup/Hold Check:** The arrival times at sequential elements are compared to clock timing requirements.

Key Considerations:

Critical Path Analysis (CPA):

- The critical path is the path with the longest delay from input to output.
- In sub-nm designs, interconnect RC delays often dominate over gate delays, making accurate interconnect modeling essential.

Corner Analysis:

- STA traditionally uses “corners” representing combinations of process, voltage, and temperature extremes (PVT).
- Example: A slow-slow process corner with high temperature and low voltage may reveal potential timing violations.

Limitations in Sub-nm Designs:

- STA assumes **fixed delays**, which ignore probabilistic variations due to random dopant fluctuations and line-edge roughness.
- It does not model **signal integrity effects**, such as **crosstalk**, where adjacent signal transitions induce additional delay or glitches.
- **Power supply noise** (IR drop) can alter effective gate delays, which traditional STA cannot account for.

Example:

A 3 nm high-performance microprocessor may have 10,000 critical paths. STA can quickly identify the worst-case paths, but without accounting for IR drop, timing violations under peak switching activity could be missed.

Dynamic Timing Analysis

Dynamic Timing Analysis (DTA) complements STA by simulating the **temporal behavior of circuits under realistic conditions**, capturing interactions that STA cannot. DTA is especially important for sub-nm designs with high switching densities and tight timing margins.

Key Features:

- **Switching Activity:** DTA considers realistic input patterns and probabilities of transitions.
- **Crosstalk-Induced Delays:** Coupling between neighboring interconnects is modeled to account for induced noise and delay.

- **Power-Supply Noise:** Voltage droops due to switching activity are incorporated, affecting gate switching speed.

Advantages:

- Provides **more accurate delay estimation** compared to STA.
- Captures **path-dependent effects**, such as glitches and dynamic hazards, which are ignored in STA.

Challenges:

- **Computational Complexity:** Simulating all possible input vectors is infeasible for large sub-nm designs.
- **Memory Requirements:** Storing waveforms and switching probabilities for millions of gates is resource-intensive.

Practical Usage:

DTA is often used selectively for:

- Critical paths identified by STA.
- High-speed buses or timing-critical modules.
- Verification of noise- or crosstalk-sensitive regions.

Example:

In a 2 nm SoC, DTA revealed that crosstalk-induced delay added up to 15 ps on a critical bus line, which STA had missed. Designers used shielding and wire spacing adjustments to mitigate this effect.

Variation-Aware Timing

Sub-nm designs are highly sensitive to **process variations**, such as random dopant fluctuations, line-width roughness, and local temperature differences. Variation-aware timing accounts for these effects probabilistically, improving **yield prediction** and **robustness**.

Key Techniques:

Statistical Static Timing Analysis (SSTA)

- Replaces deterministic gate and interconnect delays with **probabilistic distributions**.
- Propagates statistical delays through the timing graph using convolution techniques.
- Provides **probability of timing violations** rather than binary pass/fail results.

Advantages:

- More accurate for predicting timing failures in sub-nm nodes.
- Reduces overdesign compared to conservative worst-case STA.

Monte Carlo Simulations

- Randomly samples process, voltage, and temperature variations to evaluate circuit timing.
- Helps estimate **distribution of path delays**.
- Computationally expensive but highly accurate for small critical modules.

Corner-Based Statistical Modeling

- Instead of considering only extreme PVT corners, designers define **statistical corners** that represent likely variation scenarios.
- Balances simulation accuracy and runtime.

Power Integrity Analysis

Power integrity ensures reliable voltage delivery to all parts of the IC under dynamic and static operating conditions.

IR Drop Analysis

- Voltage drops (IR drop) occur due to resistive losses in the power grid.
- High IR drop may cause **timing violations**, functional errors, and reliability issues.

Table 1: Typical IR Drop Limits for Sub-nm Designs

Voltage Node	Max Allowable IR Drop	Impact on Performance
VDD (Core)	5–10%	Timing degradation
VDD (IO)	10–15%	Functional errors

Voltage Node	Max Allowable IR Drop	Impact on Performance
VSS	5%	Noise margin

Electromigration (EM)

- EM results from momentum transfer between electrons and metal atoms.
- Sub-nm interconnects with high current density are highly prone to EM failures.

Mitigation Techniques: wider metal tracks, current-aware routing, and redundant vias.

Decoupling Capacitor Design

- Decoupling capacitors reduce transient voltage fluctuations.
- Placement optimization is crucial to maintain voltage stability across large sub-nm chips.

Noise and Crosstalk Impact

- Switching noise can propagate through shared power networks, affecting timing and functionality.
- Signal integrity-aware power grid design is essential.

Integrated Timing and Power Integrity Analysis

In sub-nm designs, timing and power integrity are **tightly coupled**. Voltage fluctuations in the power delivery network (PDN) directly affect gate delays, which in turn impact timing margins. Conversely, high switching activity can exacerbate IR drop and induce electromigration (EM) issues, threatening power integrity. Hence, analyzing timing and power integrity separately is insufficient; an **integrated co-analysis** is essential for reliable design.

Co-Analysis Methodologies

Modern sub-nm IC design flows employ **co-analysis techniques** that consider timing and power effects simultaneously.

Coupled STA & Power Integrity (PI) Tools

- Traditional STA assumes nominal supply voltage for gate delays. In reality, **IR drop** and **voltage noise** dynamically affect timing.
- **Coupled STA-PI** tools integrate power delivery models with timing analysis to calculate **voltage-aware delays**.
- Example workflow:
  1. Compute IR drop across the power grid.
  2. Update gate delays based on local voltage drops.
  3. Re-run STA with adjusted delays to detect timing violations caused by PI effects.

Benefits:

- Accurate identification of timing violations due to **power-induced delays**.
- Supports **design decisions** such as decoupling capacitor placement and grid reinforcement.

Iterative Co-Optimization Approach

An iterative approach balances timing, power integrity, and area constraints:

1. **Placement Optimization:** Place high-switching or critical cells close to power sources to reduce IR drop.
2. **Routing & Shielding:** Optimize interconnects for minimal crosstalk and reduced resistance.
3. **Decoupling Capacitor Placement:** Add capacitors strategically to stabilize local voltages.
4. **Re-analysis:** Perform timing and power integrity checks iteratively until design meets all margins.

Key Advantages:

- Ensures timing reliability under real-world voltage fluctuations.
- Mitigates excessive IR drop in hotspots.
- Reduces EM risks in high-current-density paths.

Signal-Power-Timing Awareness

Advanced co-analysis considers **signal integrity**, timing, and power simultaneously:

- Crosstalk delays in high-speed buses are modeled with dynamic voltage drop effects.
- Switching-induced noise is propagated through PDN models to adjust gate delays in STA.
- Tools like **Synopsys PrimeTime with Voltus** or **Ansys RedHawk** implement this integrated methodology for full-chip analysis.

Example Flow

A practical sub-nm design flow integrating timing and power integrity is shown below:

Step 1: Initial Placement & Routing

- Generate a preliminary netlist.
- Define floorplan, macro placement, and initial routing for power/ground networks.

Step 2: Static Timing Analysis (STA)

- Identify **critical and near-critical paths**.
- Check setup and hold timing margins under nominal voltage conditions.

Step 3: IR Drop & EM Analysis

- Analyze the **power grid** to identify voltage droops in hotspots.
- Check EM violations in high-current interconnects.
- Map IR drop results to gate delay adjustments.

Step 4: Floorplan Refinement & Power Network Adjustment

- Reinforce power grid in regions with high IR drop.
- Place additional decoupling capacitors near critical cells.
- Adjust cell placement to reduce timing and power hotspots.

Step 5: Iterative Re-analysis

- Re-run STA with voltage-aware delays.
- Re-check IR drop and EM violations.
- Repeat iterations until **timing and power integrity margins** converge to acceptable levels.

Step 6: Final Verification

- Perform **variation-aware timing** (SSTA or Monte Carlo) considering voltage fluctuations.
- Confirm **signal integrity**, crosstalk effects, and worst-case power scenarios.

Practical Example

Sub-nm 3 nm High-Performance SoC:

- **Power Grid:** Multi-VDD domains with dense decoupling capacitor insertion.
- **Critical Path Analysis:** STA identified 8,000 critical paths.
- **IR Drop Impact:** Maximum IR drop observed at 6% of VDD; without adjustment, 2% of paths would violate setup timing.
- **EM Check:** High-current paths in the ALU required wider metal layers.
- **Optimization:** Adjusted placement and added local decoupling capacitors, reducing voltage-aware timing violations to <0.5%.

Conclusion: Iterative integrated analysis prevented late-stage tape-out failures and improved overall yield and reliability.

Key Considerations for Sub-nm Designs

- **Grid Modeling:** Accurate multi-layer PDN modeling is essential to predict voltage droops and EM hotspots.
- **Dynamic Effects:** Peak switching activity may temporarily violate timing; transient analysis is needed.
- **Tool Integration:** Seamless co-analysis requires tools that can exchange **timing, voltage, and EM data** efficiently.
- **Design-for-Resilience:** Adding guard-bands, decoupling capacitors, and shielding improves both timing and power margins.
- Re-run timing analysis with updated power effects.

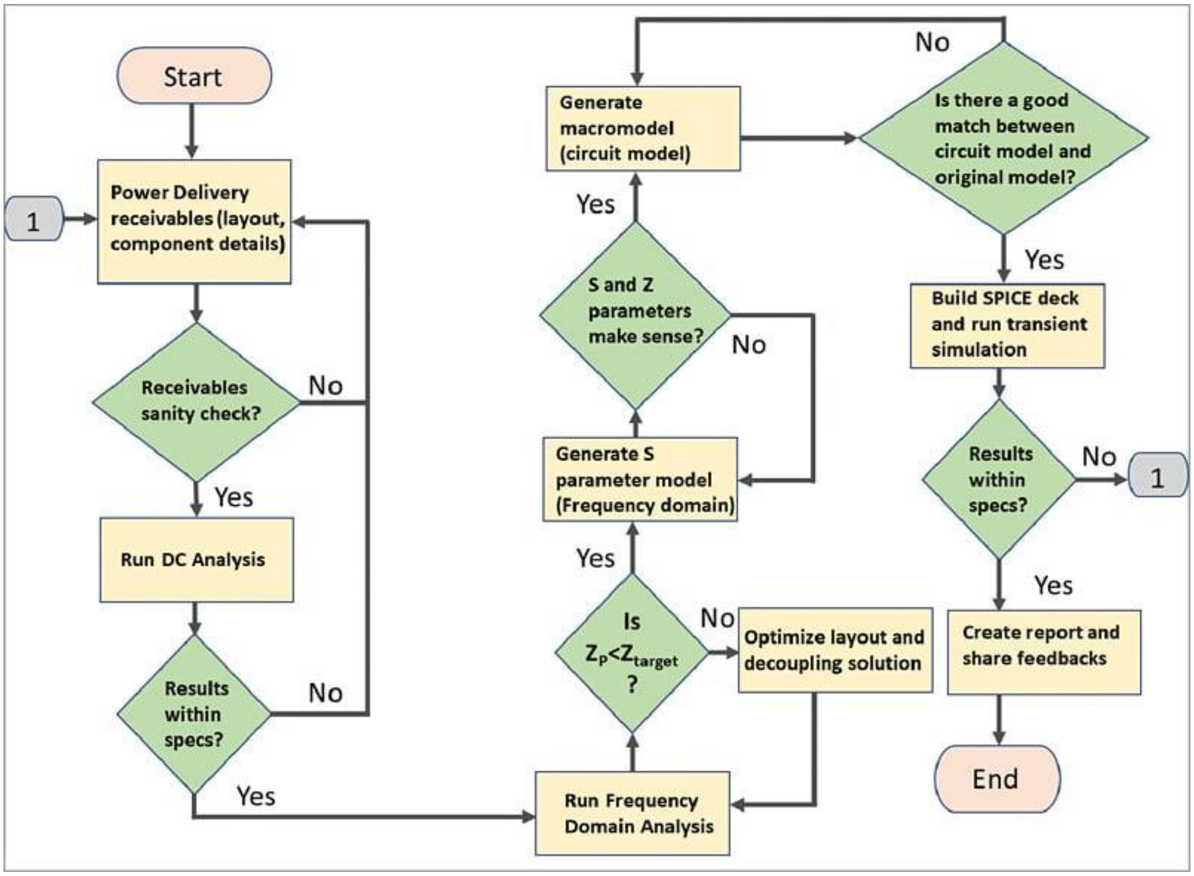

Figure 1: Integrated Timing and Power Integrity Flow

Tools and Simulation Platforms

Several commercial and academic tools assist in sub-nm timing and power integrity analysis:

Tool	Functionality	Notes
Synopsys PrimeTime	STA, SSTA	Industry standard, handles variation-aware timing
Cadence Voltus	IR drop, EM analysis	Power grid verification
Ansys RedHawk	Full-chip PI analysis	Includes dynamic and transient simulations

Tool	Functionality	Notes
OpenROAD	Academic tool for layout and timing optimization	Open-source platform for research

These tools allow designers to simulate large sub-nm designs accurately before tape-out, reducing costly design iterations.

Emerging Techniques and Trends

Machine Learning in Timing and Power Analysis

- ML models predict timing and IR drop hotspots based on layout and design metrics.
- Reduces simulation time compared to traditional iterative methods.

Adaptive Voltage Scaling

- Dynamically adjusts voltage levels based on workload, temperature, and IR drop.
- Helps maintain timing integrity while reducing power consumption.

Multi-Objective Optimization

- Timing, power, and area (PPA) optimized together using genetic algorithms, reinforcement learning, or heuristic approaches.

Case Study

Sub-nm 3nm High-Performance Microprocessor:

- **Power Grid:** Multiple VDD domains with local decoupling capacitors.
- **Timing Analysis:** SSTA used to capture process variation across 10,000 critical paths.

Results:

- Maximum IR drop: 7% of nominal VDD
- Timing violation probability reduced from 2.5% to 0.3% after iterative co-analysis.

Conclusion: Integrated timing and power integrity analysis significantly improved yield and reliability.

Conclusion

Sub-nm IC designs present significant timing and power integrity challenges due to scaling, variability, and high current densities. Effective design requires **variation-aware timing analysis**, **robust power grid design**, and **co-optimization strategies** that consider both timing and power effects. Emerging methodologies, including machine learning and multi-objective optimization, promise to further improve design reliability, performance, and yield. Designers must adopt integrated workflows and simulation-driven approaches to meet the stringent demands of sub-nm technology nodes.

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