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The Convergence of Communication Systems and Computing with VLSI Technology

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Abstract

In this paper, the increasing convergence of communication systems with computing, and how this trend is going to continue, is highlighted. According to Moore's law, the number of transistors used in a given area doubles every 18 months. This means that within 18 months, you can expect communication technology to move to the next level, and that's why we are experiencing such a fast-paced information revolution nowadays. The balance between telecom and power distribution is essential to enable this distribution. This paper will highlight the convergence of computing and data communications as well as the essential power management architecture that keeps it going.

Keywords: *VLSI Communication, Telecom and Computing,* VLSI based *Convergence*

INTRODUCTION

The convergence of computing and communications- "Commputing"-is happening both on the signal and the power path, creating new opportunities as well as challenges for designs. Silicon integration of computing, communications, and wireless functions on the same die, or on the same process technology, is blurring the lines between computing and communications. Powering this silicon requires a good understanding of a new environment that does not conform well to traditional schemes and classifications.

THE PROLIFERATION OF POWER SUPPLIES

The two end points in the power chain are the "load" and the "wall power." The load end of the chain is in constant evolution,

resulting in continuous changes that generate new opportunities and new challenges. The technology driver on the load side is ultimately Moore's law. Doubling the number of transistors per a given area every 18 months creates a technology hierarchy by which the CPU-at the top of the food chain-is designed with the smallest minimum feature (90 nm in 2004-5) and requires the lowest supply voltages (1-1.5 V). Consequently, the previous generation fab infrastructure at 130 nm gets recycled down the food chain for the next high protein product-say memory-that gets powered at voltages around 2.5 V or lower. This cycle goes on and on. As the performance of such loads (e.g., CPUs, memories, chipsets) tends to go up while voltage decreases, the end result is an increase in power (Watts) demand. When such a load, say a CPU, is part of a computing system, it gets powered by a voltage regulator.

The voltage regulator typically is referred to as voltage regulator module if the power supply is a module plugging into a socket on the motherboard, or Voltage Regulator Down (VRD) if the same circuitry is built-in permanently "down" on the motherboard. When the same load is part of a communications system, it will be powered essentially by the same regulation electronics, now called the Point of Load regulator or simply POL. On the wall power side we have two different power distribution systems: the 48 V power for telecom systems and the AC line (1 10 V or 220 V AC) for computing. Figure 1 illustrates and compares the two systems.

TELECOM POWER DISTRIBUTION

Traditionally, telecom systems (Figure 1a) have distributed DC power (48 V typically) obtained from a battery backup that is charged continually by a rectifier charger from the AC line.

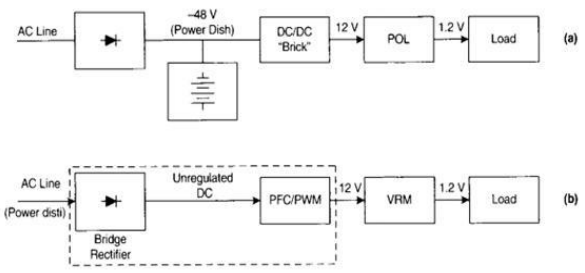

Figure 1 (a) Telecom versus (b) Computing power distribution system.

This is the case for the power distribution in land telephones for example. Subsequently, this 48 V (in reality a voltage spreading from 36 V to 72 V) is converted into various low positive DC voltages (Figure 1a shows 12 V only for simplicity). This down conversion generally is accomplished by isolated DC-DC converters referred to as bricks, although non-isolated buck converters are sometimes used in telecom. Isolation in bricks is driven by a number of technical factors, including cleaner ground loops, ease of handling the wide input to output voltage ratios (easily 10: 1) by means of the transformer turn ratio, and inherently good over-voltage protection of the load due to the low voltage at the output of the transformer. Such a 12 V (or 5 V) bus may then be reduced down to the final voltage rails (3.3 V, 2.5 V, 1.2 V, etc.) by means of a DCDC converter for each rail or even one for each single load, depending on the overall power management scheme. This type of low voltage DC-DC converter is referred to as point of load in telecom systems.

COMPUTING POWER DISTRIBUTION

In a typical computing system (Figure 1b), such as a desktop PC, the power is drawn from the AC line. After rectification (AC to unregulated DC voltage conversion), the high input voltage is "bucked" down to the standard 12 V, 5 V, and 3.3 V busses by the PFC and PWM block. The silver box inside the PC box performs the down conversion. These voltages are then delivered by a cable to the motherboard, where they are reduced to the final voltage rails by VRMs, VRDs, and other types of voltage regulators.

MULTIPHASE BUCK CONVERTER FOR POLS AND VRMS

POLs and VRMs essentially are modules and come in a number of moreor-less standard form factors. Standardization and modularization differentiate these elements and make them specific to the application at hand, but at their heart they are powered by similar technologies and architectures. Their similarity derives from the fact that they are powering similar or identical loads from similar or identical input voltages. The most popular architecture for step-down regulators, from 12 V or less to any voltage down to I V or less, is the non-isolated, multiphase interleaved buck converter. The buck

converter is a very popular and resilient architecture, thanks to its simplicity and effective Interleaved multiphase is the feature that has given a new lease on the life of this architecture.

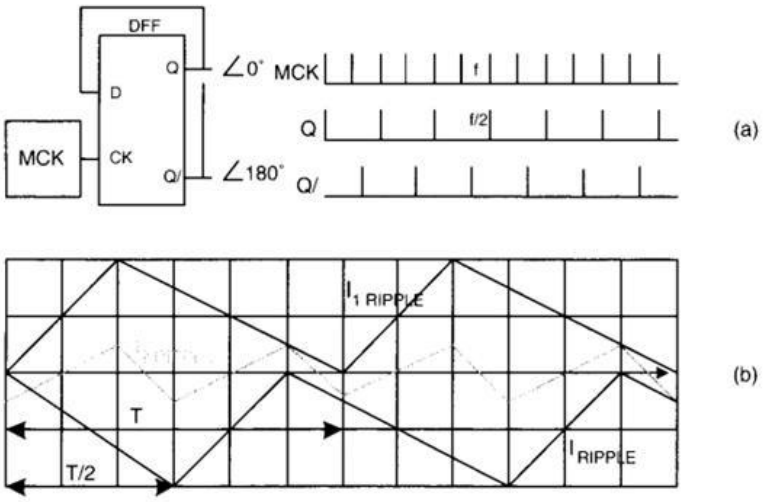

Figure 2 Two-phase interleaved (a) buck converter and (b) output ripple current waveforms

Multiphase refers to paralleling of two or more buck converters, and interleave signifies the time spacing of the clock cycles between the converters. Figure 2 refers to two buck converters (or two slices or phases of a multiphase buck converter) working in opposition of phase. In Figure 2(a), the two clocks in phase opposition are generated at the output of a logic device (see glossary), starting from a master clock (MCK). The currents in each phase have very high DC components and a small ripple on top of such DC interleave is all about reducing that ripple amplitude even more, as the ripple represents noise or deviation from an ideal direct current waveform. Hence in this discussion we ignore the DC components and focus only on the variable content, or ripples called

I*,R,pp,, and in Figure 2(b). In the same Figure 2(b), 12QRIppLE is the resulting ripple current after the currents in the two slices are summed. The interleave produces these fundamental benefits:

- Effective operation at twice (or n times for n slices) the single slice frequency without the switching losses associated to high frequency of operation.
- Smaller output ripple as demonstrated graphically in Figure 2(b) by the

smaller amplitude of the resulting ripple compared to the amplitude of the ripple components. On the other hand, instead of working toward a smaller ripple, this architecture can be utilized to maintain a specified ripple with smaller and hence cheaper output components (inductors and capacitors).

The higher duty cycle and higher on-time is demonstrated in Figure 2(b) by the longer duration of the positively sloped segments in the resulting ripple compared to the ripple components. Higher on-time means lower peak currents within a clock cycle. Since the on-time is the time during which current is drawn from the input capacitors, lower peak currents lead to savings in input capacitors as well. An issue that needs attention when it comes to interleaved schemes is phase current balancing, or the need to assure that all phases carry an identical amount of current. This can be accomplished in many ways, from simple ballast schemes to active current sensing and balancing.

EFFICIENT POWER MANAGEMENT ICS TAILORED FOR D D R-S D RAM MEMORIES

A new type of Single Data Rutidom Access Memory (SDRAM), Double Darn Rate (DDR) DDR-SDRAM for short, has gained popularity in desktop and portable computing thanks to its superior performance (initially 266 Mbps data rate versus 133 Mbps data rate for plain SDRAM) and low power dissipation at a competitive cost when compared to competing memory technologies. Subsequently, the DDR data rate has increased to 400 Mbps.

A second generation DDR, or DDR2 (JESD79- 2A), has been introduced recently, extending the data rate from 400 up to 667 Mbps. DDR memories require a new and more complex power management architecture in comparison with the previous SDRAM technology. This paper reviews the power requirements for DDR-SDRAM memories, covering static, transient, and stand-by modes of operation. Alternative schemes of power management are discussed and an example of a complete power management system, based on efficient switching voltage regulation, is provided. Finally, future trends in power management for DDR-SDRAM memories are examined.

DDR POWER MANAGEMENT ARCHITECTURE

Figure 3 illustrates the basic power management architecture for first generation DDR memories. In DDR memories the output buffer is a push-pull stage, while the input receiver is a differential stage. This requires a reference bias midpoint VREF and, consequently, an input voltage termination capable of sourcing, as well as sinking, current. This last feature (sourcing and sinking current) differentiates the DDR V, termination from other terminations present in the PC motherboard, noticeably the termination for the Front System Bus (FSB), connecting the CPU to the Memory Chatzriel Hub (MCH), which requires only sink capability due to termination to the positive rail. Hence, such DDR Vn termination cannot reuse or adapt previous V, termination architectures and requires a new power design.

In first generation, DDR memories the logic gates are powered by 2.5 V. Between any output buffer from the chipset and the corresponding input receiver on the memory module, typically we find a routing trace or stub, that needs to be properly terminated with resistors RT and RS as indicated in Figure 3. When all the impedances, including that of the output buffer are accounted for, each terminated line can sink or source k 16.2 mA. For systems with longer trace lengths between transmitter and receiver, it may be necessary to terminate the line at both ends, doubling the current.

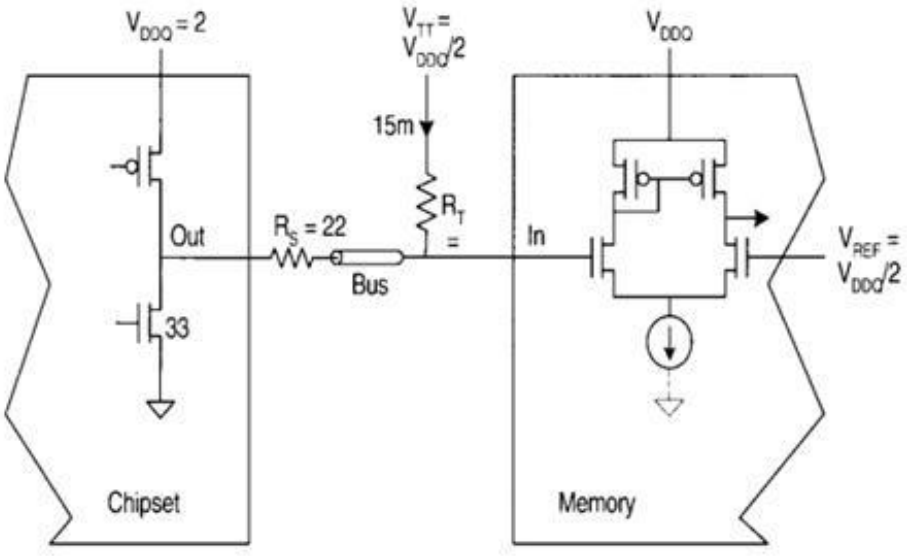

Figure 3 Illustration of DDR power supply architecture.

The 2.5 V VDDQ required for the DDR logic has a tolerance of +200 mV. To maintain noise margins, DDR termination voltage, V_{TT}, is required to track V_{DDQ}. It must be equal to $V_{DDQ}/2$, or approximately 1.25 V, with an accuracy of plus or minus three percent. Finally, the reference voltage, V_{REF}, must be equal to V_{TT} to +40 mV. These tracking requirements, plus the requirement that V, can both sink and source current, are the features that present the unique challenges of powering DDR memory.

CONCLUSION

The convergence of computing and communications brings together two cultures and, in fact, two separate power systems, and classifications. Power distribution at the source starts very differently for these two fields, but at the point of load there is clear convergence. When we dig below the surface of VRMs and POLS, we find the same technologies and architectures at play and between the latter, the interleaved buck converter rules.

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