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An Analytical Delay and HSPICE Analysis in RLC Modeled High Speed On-Chip VLSI Interconnect

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Abstract

An analytical delay model is proposed for RLC modeled high speed on-chip VLSI interconnects based on a second order approximate transfer function in DSM technology environment. The proposed analytical delay model is almost independent of the ratio of V_o/V_i (output voltage to input voltage) and the driver resistance (R_D) has an impact on the delay correspondingly speed and reliability of the circuit gets affected. It is observed that real pole model provides better accuracy and is much faster than the complex pole model. An analytical delay model for RLC interconnect line with complex and real poles based on a second order approximation that considers the effect of inductance and incorporates ground capacitance. The impacts of driver/source resistance and output load capacitance have also been taken into account. For a wide range of driver, load, and interconnect line parameters the delay of the circuit model is calculated. It is observed that the average error rate of our developed models (both real and complex pole models) is within 10.49% and 10.14% with HSPICE simulation.

Keywords-*Delay model, Transfer function, RLC Interconnect, complex poles, real poles*

INTRODUCTION

The integrated circuit industry has been pursuing Moore's curve down to deep submicron (DSM) and ultra deep submicron (UDSM) technology environment that led to the anticipated

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delivery of 100 billion transistors on a 300 mm2 die with less than 1V power supply at GHz frequency range [1]. However, conventional 2-D integration of these enormous numbers of transistor on a single substrate would not provide the expected improvements in terms of functionality, reliability, and performance. 3-D ICs have evolved as the most potential future direction to increase the integration capacity of MOS devices and facilitate integration of heterogeneous materials, devices, and technologies based on silicon, group III–V semiconductors, carbon nanotubes, graphene, and other 2-D nanomaterials [3]–[5]. However, the grand challenge is to reliably and efficiently take the full advantage of the unprecedented computing power offered by the billions of transistors on a single chip.

Electrical interconnects, which will remain the primary medium of signal communication in all existing and emerging IC technologies, are limited by RLC parasitic effects. All the investigations and predictions indicate that the overall signal propagation delay will be governed by the interconnect delay in the scaled ICs, and interconnect centric limitations would prevent us from taking the full advantage of what nanoscale technology can offer. Inductances, which were ignored in earlier designs, cannot be disregarded due to the longer length of wire and the higher signal frequencies in extremely dense ICs [6], [7]. Inductance, which is more prominent in the wider top-layer interconnect lines used for clock and global signal distribution, introduces various anomalies like oscillation, overshoot, and ringing in signal waveform and electromagnetic interference in the ICs. As a consequence, both signal delay and noise would increase with higher inductance [2]. Therefore, accurate and efficient modeling and estimation of R LC interconnect para- meters are very critical for high performance ICs.

Modeling and analyzing interconnect parasitic elements are fundamen- tally difficult from a computational point of view due to the 3-Deffects inside complex ICs. Including inductance makes it further complicated. Therefore, both accuracy and efficiency are equally important in interconnect modeling and signal propagation characterization. Accuracy of the estimation of inductive effects is essential for correct output realization and the quantification of the impact of inductance on distributed R LC interconnect and circuit behavior at higher frequency.

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Existing well-established R LC interconnect analysis techniques are based on either analytical or simulation methods. Simulation methods, such as full circuit SPICE/HSPICE simulation, give the most accurate understanding of the behavior of random interconnect configurations. However, computationally this method is expensive and is not feasible at all stages of design hierarchy. Consequently, the analysis of lossy interconnect structures have been done by utilizing the convolution technique and faster analytical methods based on moment computation [8], [9], [16]–[21].

In addition, complex frequency hopping [30], asymptotic waveform evaluations [31], cascaded ABCD matrixes [32], scattering parameter macromodels [33], effective lumped resistance and capacitive models [34], methods of characteristics [35], and rational approximation model (such as PRIMA [36], MRA [37], [38], and compact differences [39]) are being used to investigate and model the propagation delay of interconnect lines. These techniques are computationally too expensive to be used throughout the repetitive layout and/or circuit optimization process.

Efficient but highly inaccurate methods like Elmore propagation delay model are widely being used for delay analysis at the initial stages of the IC design. The Elmore delay model gives the RC delay of the interconnect line that signifies the first pole of the transfer function in the Laplace domain. However, the Elmore delay cannot estimate the propagation delay for the R LC interconnect lines for which inductive impedance effects cannot be ignored [22].

For analysis including inductance, an approach based on moment matching is better [44], [45]. For faster analysis, including a lower number of moments is necessary. However, a lower number of moments lead to higher errors. During the initial design steps, it is often necessary to quickly estimate and monitor the anticipated performance. In these cases, a faster approach with a minimum number of moments will be very valuable. However, one of the main limitations of [44] and [45] is that this approach did not consider the ground capacitance in the estimation of the propagation delay.

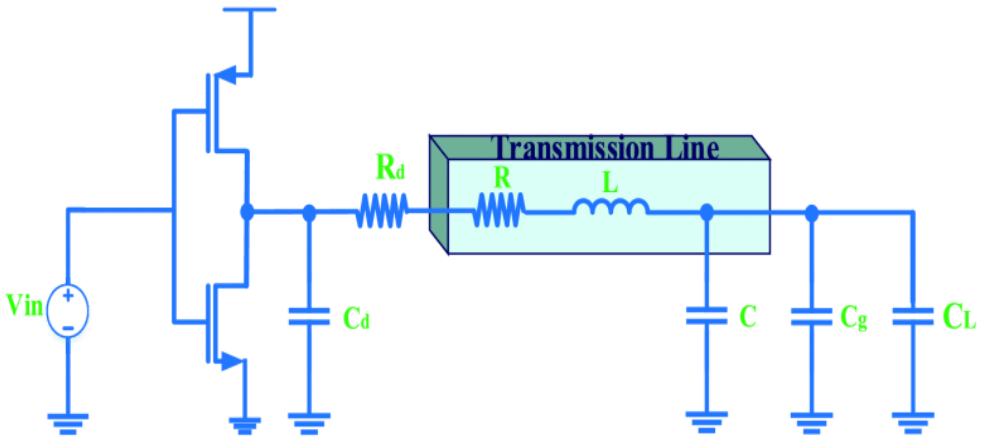
In fact, it was not that significant 20 years back when operating frequencies were lower. We proposed a way to overcome this limitation through complex pole [1]

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and real pole [28] scenarios-based analysis of interconnect line. We introduced a new time delay model ([1] and [28]) based on second order approximation in a single R LC interconnect line without considering the impact of ground capacitance on interconnect delay. Therefore, the primary objective of this paper is to introduce a novel mathematical approach to model the propagation delays in distributed R LC interconnect lines including inductance and ground capacitance with a constant power supply (Vdd). The proposed model is based on simple quadratic equation that represents the first and the second poles of the transfer function in the Laplace domain, where a pole can be either real or complex for a specific interconnect structure. The proposed model would help to accurate the characterization of output response in R LC interconnect networks. Characterization of output response is critical, because it has serious implications on signal integrity, performance, and other aspects of ICs and systems.

We have also demonstrated how the proposed propagation delay model can be used in interconnect analysis. More specifically, we have explained how to select the values of a and b to achieve higher accuracy of the proposed models for real and complex poles cases. To validate our investigation and proposed delay models, HSPICE simulation results using different inter- connect structures with a variety of interconnect parameters, driver resistances, and load capacitances are presented.

Interconnect Model



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The circuit in figure (1) shows an LTI system whose response in time domain can be calculated from the Inverse Laplace transform of the LTI system. The transfer function of the LTI system of one RLC segment is as

$$H(s) = \frac{1}{(1 + R_D C_T s)cosh\theta + \left(\frac{R_D}{\sqrt{\frac{1+sL}{sC}}} + \sqrt{\frac{1+sL}{sC}} C_T\right) sinh\theta} \quad (1)$$

Where R_D is the driver resistance, total capacitance$C_T = C_g + C_l$, and $\theta = l\sqrt{((R + sL)sC)}$. The value of C_g is

$C_g = \varepsilon\,[(w/h) + 2.22((s/s + 0.7h))^{3.19} + 1.17(s/s + 1.51h)^{0.76}\cdot(t/t + 4.53h)^{0.12}]$

The transfer function in equation (1) can be approximated as

$$H(s) \cong \frac{1}{1 + C_1 s + C_2 s^2} \quad (2)$$

Where the coefficients are $C_1 = R_d C_T + (l^2/2)RC + lR_d C + lRC_T$ and $C_2 = (l^2/2)(R_d C_T RC + LC) + lLC_T$, respectively

A) Complex pole model: $C_1^2 - 4C_2 < 0$

The output for step input response is calculated as for two dominant poles

$$V_o(t) = \frac{V_{dd}}{p_1 p_2}\left(1 - \frac{p_2}{p_2 - p_1} e^{p_1 t} + \frac{p_1}{p_2 - p_1} e^{p_2 t}\right) \quad (3)$$

Where $p_1 = a + jb\ ;\ p_2 = a - jb$ *and the value of* $a = \frac{C_1}{2C_2}; b = \frac{\sqrt{C_1^2 - 4C_2}}{2C_2};\ \theta = tan^{-1}\left(\frac{b}{a}\right)$

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Delay is calculated by solving following equation recursively in time

$$e^{at}sin(bt+\theta) = b(1 - (a^2+b^2)V_{th}) \quad (4)$$

V_{th} is the output to input ratio voltage. The time delay for complex poles

$$\tau_c = \frac{1}{b}\left[sin^{-1}\left(be^{-aT_{ED}}(1-(a^2+b^2)V_{th})\right) - tan^{-1}\frac{b}{a}\right] \quad (5)$$

Where $T_{ED} = R_D(C+C_T) + R\left(\left(\frac{C}{2}\right)+C_T\right)$ is the Elmore's delay.

B) **Real Pole model:** $C_1^2 - 4C_2 > 0$ the output response for the case of two different real poles in time domain is as:

$$V_o(t) = \frac{V_{dd}}{p_1p_2}\left(1 - \frac{p_2}{p_2-p_1}e^{p_1t} + \frac{p_1}{p_2-p_1}e^{p_2t}\right) \quad (6)$$

Where $p_1 = \left(\frac{-C_1+\sqrt{C_1^2-4C_2}}{2C_2}\right)$ and $p_1 = \left(\frac{-C_1-\sqrt{C_1^2-4C_2}}{2C_2}\right)$

Since $|p_2| >> |p_1|$ so contribution of $\frac{p_1}{p_2-p_1}e^{p_2t}$ is neglected.

$$V_o(t) \approx \frac{V_{dd}}{p_1p_2}\left(1 - \frac{p_2}{p_2-p_1}e^{p_1t}\right) \quad (7)$$

Therefore, the delay τ_r for real pole

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$$\tau_r = \frac{1}{p_1} ln \left[\frac{(p_2 - p_1)}{p_2} (1 - p_1 p_2 V_r) \right] \quad (8)$$

CONCLUSION

From HSPICE simulation, it is noticed that delay increases significantly with the increase of inductive effect. Our developed model also shows the same trends. However, the most significant conclusions we can make from these results and observations are as follows: 1) the real pole based delay model is much faster compared to the complex pole-based model; 2) the driver resistance has a significant contribution in making a transition from the real pole model to the complex pole model and vice versa; and 3) the output response of the real pole model-based transfer function shows better accuracy than the complex pole model-based transfer function. The last observation would help optimize the parasitic values of the interconnect line to achieve faster operation. Although these models consider only two poles, it is believed that the resulting delay is a good estimation for an early stage analysis during the long iterative design and layout synthesis processes of high density ICs. The proposed delay models can be embedded as a quick tool in the CAD flow of IC designs.

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