

RISC-V ISA Optimization for Embedded Workloads

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Abstract

RISC-V is an emerging open-source instruction set architecture (ISA) that has gained significant traction in the embedded systems domain due to its modularity, simplicity, and extensibility. As embedded workloads become more diverse and performance-constrained, optimizing the RISC-V ISA for such applications is critical to achieving low power consumption, high performance, and area efficiency. This review paper explores the current strategies for RISC-V ISA optimization targeted at embedded workloads. We examine architectural enhancements, instruction set extensions, compiler-level optimizations, and hardware-software co-design approaches. Additionally, we discuss case studies demonstrating energy efficiency improvements and performance gains in real-world embedded applications. Challenges, trade-offs, and future directions are also highlighted, providing a comprehensive reference for researchers and engineers working on RISC-V embedded systems.

Keywords: *RISC-V, Embedded Systems, ISA Optimization, Instruction Set Extensions, Low Power, Performance Tuning, Compiler Optimization, Hardware-Software Co-Design*

1. INTRODUCTION

Embedded systems have become ubiquitous in modern electronics, ranging from IoT devices, wearable technologies, automotive control units, to industrial

automation systems. These systems are typically resource-constrained, requiring careful optimization of computing, energy, and memory resources. The choice of instruction set architecture (ISA) plays a

vital role in determining the overall efficiency of these systems.

RISC-V is a novel open-source ISA designed with simplicity, modularity, and scalability in mind. Unlike proprietary ISAs such as ARM or MIPS, RISC-V allows customization of base and extended instruction sets to suit application-specific requirements. This flexibility is particularly valuable for embedded workloads, where energy efficiency and performance are often competing constraints.

Optimizing RISC-V for embedded workloads involves multiple layers: hardware-level enhancements (e.g., custom functional units), ISA-level modifications (e.g., custom instructions), compiler optimizations, and system-level considerations. This paper reviews these strategies, highlighting the trade-offs, benefits, and practical implementations.

2. BACKGROUND: RISC-V ARCHITECTURE AND EMBEDDED WORKLOADS

Embedded systems present unique challenges that distinguish them from general-purpose computing. These systems often operate under strict constraints for power, memory, and real-time performance, making the underlying processor architecture a critical factor in achieving optimal system efficiency. RISC-

V has emerged as a promising candidate for embedded applications due to its simplicity, modularity, and adaptability. This section provides a detailed background on RISC-V ISA and the characteristics of embedded workloads, which guide optimization strategies.

2.1 Overview of RISC-V ISA

RISC-V (Reduced Instruction Set Computing – Five) is an open-standard instruction set architecture designed to provide a clean, extensible, and efficient computing platform. Unlike traditional proprietary ISAs such as ARM or x86, RISC-V emphasizes simplicity, regularity, and modularity, allowing developers to customize processors for specific application needs, which is especially valuable in embedded domains.

The architecture is organized into three main components:

1. Base ISA

The base ISA provides a minimal set of instructions necessary to run general programs. It is available in multiple word lengths:

- **RV32I** – 32-bit integer instructions suitable for microcontrollers and low-power embedded devices.
- **RV64I** – 64-bit integer instructions for higher-performance embedded processors and mid-range applications.

- **RV128I** – 128-bit variant, designed for future high-performance computing but less common in current embedded systems.

The base ISA includes essential operations such as arithmetic, logical, branch, load/store, and control instructions. Its simplicity reduces decoding complexity and enables efficient pipeline implementations, which is beneficial for low-power, resource-constrained systems.

2. Standard Extensions

RISC-V provides optional extensions to the base ISA, allowing designers to tailor the processor for specific workloads:

- **F (Floating-point extension):** Supports single-precision floating-point operations, useful for signal processing or lightweight scientific calculations.
- **D (Double-precision floating-point):** Optional for more complex numerical computations.
- **A (Atomic extension):** Enables atomic memory operations critical for multi-core embedded systems.
- **C (Compressed instructions):** Reduces instruction size from 32-bit to 16-bit, decreasing code memory footprint and improving instruction cache efficiency.
- **V (Vector extension):** Introduces vectorized operations for parallel data

processing, suitable for embedded ML or DSP tasks.

3. Custom Extensions

Beyond standard extensions, RISC-V allows **user-defined custom instructions** to accelerate application-specific workloads. For example:

- Digital Signal Processing (DSP) accelerators for audio or sensor data.
- Cryptographic accelerators for secure IoT communication.
- Matrix or convolution operations for embedded machine learning.

These customizations enable significant performance improvements without requiring a completely new processor design.

Advantages for Embedded Systems:

1. **Modularity:** Designers include only the necessary extensions for the target application, reducing power consumption and silicon area.
2. **Open-source:** The ISA is free to use and modify, lowering the cost of hardware implementation and encouraging community-driven enhancements.
3. **Scalability:** RISC-V can scale from ultra-low-power microcontrollers to high-performance embedded processors, allowing a consistent software ecosystem across different device classes.

Example: A low-power sensor node might use RV32I with the C extension to minimize memory and energy usage, whereas an embedded vision processor could employ RV32I with V (vector) and custom convolution instructions to accelerate ML inference.

2.2 Embedded Workloads Characteristics

Embedded workloads differ significantly from general-purpose computing tasks, which often prioritize raw performance. The following characteristics define typical embedded workloads:

1. **Low Memory Footprint:** Embedded systems often have limited RAM and flash memory. Programs must be compact, requiring instruction set optimizations such as compressed instructions (RVC) and efficient memory access patterns.
2. **Frequent Integer and Logical Operations:** Most embedded applications, such as sensor data processing, control loops, and state machines, rely heavily on integer arithmetic rather than floating-point computation.
3. **Limited Floating-Point Usage:** While some embedded systems require floating-point support (e.g., audio or image processing), many low-power

devices avoid it due to higher energy costs. Custom or software-emulated floating-point operations are common.

4. **Real-Time Performance Constraints:** Embedded systems frequently operate in real-time environments where predictable execution timing is critical, such as automotive control units, robotics, or medical devices. Instruction-level optimization, pipeline efficiency, and hardware loop support help meet these timing requirements.
5. **Power and Energy Efficiency Requirements:** Energy consumption is often the primary constraint in battery-powered or energy-harvesting systems. ISA-level optimizations, low-power functional units, and efficient memory access patterns directly impact energy usage.

Optimizing RISC-V for embedded workloads involves carefully selecting appropriate extensions, pipeline depth, and memory hierarchies.

For instance, enabling the compressed instruction set (RVC) reduces code size, improving instruction cache utilization and lowering energy consumption. Adding hardware loops or custom instructions for repetitive tasks can enhance performance without increasing power overhead significantly.

Example: Consider a wearable health-monitoring device that continuously collects and filters sensor data. Using RISC-V RV32I with C extension and a custom MAC instruction for filtering operations can reduce execution cycles and power consumption simultaneously.

In summary, the combination of RISC-V's modularity, extensibility, and simplicity makes it a highly suitable platform for embedded workloads. Understanding both the ISA and the unique demands of embedded applications is essential for designing optimized systems.

3. ISA-LEVEL OPTIMIZATION TECHNIQUES FOR EMBEDDED WORKLOADS

Optimizing RISC-V for embedded workloads requires careful consideration of the instruction set, as these workloads often involve resource-constrained environments with strict latency and energy requirements. ISA-level optimizations improve code density, reduce execution cycles, and enhance energy efficiency without requiring major hardware redesigns.

This section explores four prominent techniques: compressed instructions, custom instructions, hardware loop support, and vector extensions.

3.1 Compressed Instructions (RVC Extension)

The **RISC-V Compressed (RVC) extension** reduces 32-bit instructions to 16-bit equivalents. By encoding frequently used instructions in fewer bits, RVC decreases program memory usage and improves instruction cache performance—a critical factor for embedded systems with limited on-chip memory.

Key Advantages:

1. **Memory Footprint Reduction:** Studies show RVC can reduce code size by 20–30%, freeing memory for additional functionality or reducing external memory usage.
2. **Energy Savings:** Smaller instruction size leads to fewer memory fetches, reducing dynamic power consumption in instruction caches and buses.
3. **Performance Improvement:** By improving cache utilization and reducing fetch/decode overhead, RVC can increase overall execution efficiency in tightly constrained systems.

Example:

- **Load/store operations:** Compressed variants reduce instruction fetch time for repeated memory accesses.

- **Branch instructions:** Frequently used in loops, branch instructions benefit from reduced fetch and decode cycles.
- **Arithmetic operations:** Simple addition, subtraction, or logical instructions can be executed using 16-bit encodings, maintaining functionality while improving code density.

Illustration: In an IoT temperature sensor firmware, enabling RVC reduced program memory usage by 25% and decreased execution cycles for key routines by 10%, improving both energy efficiency and responsiveness.

3.2 Custom Instructions

Embedded workloads often include repetitive or computationally intensive tasks that can benefit from **application-specific instructions**. RISC-V supports the addition of custom instructions, enabling hardware accelerators to directly execute these tasks in fewer cycles.

Applications:

- **Digital Signal Processing (DSP):** MAC (multiply-accumulate) operations for filtering or FFT computation.
- **Cryptography:** Single-cycle instructions for AES, SHA, or elliptic curve computations improve security without major overhead.

- **Image Processing:** Pixel-wise operations or convolution kernels can be accelerated using specialized instructions.
- **Neural Network Inference:** Custom instructions for matrix multiplications and activations improve inference latency and energy efficiency.

Case Study:

- An IoT sensor node implemented a single-cycle MAC instruction for signal filtering.
- **Result:** DSP workload latency was reduced by ~40%, enabling faster processing of sensor data while reducing overall energy consumption.

Insight: Custom instructions reduce the number of sequential operations, eliminating pipeline stalls and unnecessary instruction fetches, which is particularly beneficial in deeply embedded real-time applications.

3.3 Hardware Loop Support

Many embedded workloads involve **repetitive loops**, such as sensor data processing, control algorithms, or audio/video filtering. Traditional loops rely on branch instructions, which introduce pipeline hazards and branch penalties. Hardware loop support addresses these issues by implementing loop counters and automatic branching directly in hardware.

Benefits:

1. **Reduced Instruction Fetch and Decode Overhead:** Hardware loops remove the need for explicit loop counter increments and conditional branches.
2. **Increased Pipeline Efficiency:** By eliminating branch instructions, pipeline stalls are minimized, improving execution throughput.
3. **Lower Energy Consumption per Iteration:** Fewer instructions executed per loop iteration reduces switching activity and memory accesses.

Example:

- A motor control algorithm in an embedded robotic arm repeatedly executes a PID controller loop.
- Using hardware loop support reduced instruction cycles by 15–20%, enabling faster control updates with less energy consumption.

Note: Hardware loops are especially effective when combined with compressed instructions, as they further reduce instruction memory accesses and pipeline stalls.

3.4 Vector Extensions (RVV)

The **RISC-V Vector Extension (RVV)** introduces vectorized instructions that operate on multiple data elements simultaneously, similar to SIMD (Single

Instruction, Multiple Data) architectures. RVV is particularly useful for embedded applications involving **machine learning, signal processing, and multimedia processing**.

Key Advantages:

1. **Parallel Computation:** RVV allows multiple arithmetic or logical operations to be executed in parallel, reducing execution cycles for data-parallel workloads.
2. **Reduced Execution Cycles for Convolution/Filtering Tasks:** Vectorized convolution in image or audio processing can execute in fewer instructions, improving latency.
3. **Energy Efficiency:** Fewer instructions per operation lead to lower instruction fetches and decreased memory traffic, conserving energy.

Example:

- In an embedded ML application performing convolutional neural network inference on sensor images:
- RVV vectorized multiply-add operations reduced total execution cycles by 50%.
- Energy per inference decreased by ~30%, demonstrating the efficiency of vectorized embedded processing.

Integration Tip: RVV works best when combined with compiler support for automatic vectorization, enabling high-

level C or C++ code to efficiently map onto vector instructions.

4. COMPILER-LEVEL OPTIMIZATION

While ISA-level optimizations directly improve the processor's execution efficiency, **compiler-level optimizations** play a critical role in translating high-level code into efficient machine instructions. In embedded RISC-V systems, where resources like memory, power, and execution time are limited, compilers can significantly enhance performance by leveraging instruction scheduling, loop transformations, inlining, and profile-guided optimizations. These techniques work synergistically with ISA-level features, such as compressed instructions and vector extensions, to maximize the efficiency of embedded workloads.

4.1 Instruction Scheduling

Instruction scheduling is a compiler optimization technique that **reorders instructions to minimize pipeline hazards** and maximize instruction-level parallelism (ILP). In modern RISC-V cores, pipelines typically include stages such as fetch, decode, execute, memory access, and write-back. Improper ordering of instructions can result in **stalls**, where the

processor waits for data dependencies to resolve, increasing execution time and energy consumption.

Key Benefits for Embedded RISC-V Systems:

1. **Fewer Stalls:** By rearranging independent instructions between dependent instructions, the compiler reduces pipeline bubbles.
2. **Reduced Energy Consumption:** Fewer stalls mean less wasted switching activity, lowering dynamic power.
3. **Better Real-Time Performance:** Predictable instruction execution ensures embedded systems meet tight timing constraints.

Example:

- Consider a sequence of instructions where a load from memory is followed immediately by an arithmetic operation using the loaded value. Without scheduling, the arithmetic instruction stalls while waiting for the memory load to complete.
- An optimized instruction schedule inserts independent instructions (e.g., computations not dependent on the load) between the load and arithmetic operation, keeping the pipeline busy and reducing overall cycles.

Embedded Case: In a low-power IoT sensor node performing continuous signal filtering, instruction scheduling reduced execution stalls by ~15%, directly improving both throughput and energy efficiency.

4.2 Loop Unrolling and Function Inlining

Embedded workloads often rely on **tight loops** for processing sensor data, controlling actuators, or performing signal transformations. Compilers can optimize these loops and function calls using **loop unrolling** and **function inlining**.

Loop Unrolling

Loop unrolling replicates the body of a loop multiple times to reduce the overhead associated with branch instructions and loop control logic.

Advantages:

- **Reduced Branch Overhead:** Fewer iterations mean fewer branch instructions, reducing pipeline stalls.
- **Increased ILP Opportunities:** Multiple operations in the unrolled loop can be scheduled in parallel.
- **Trade-off:** Increased code size, which may be a concern in memory-constrained embedded systems.

Example:

- A FIR (Finite Impulse Response) filter in an embedded audio application involves a loop applying multiply-accumulate operations across 16 samples.
- Unrolling the loop 4 times reduces branch instructions by 75% and allows simultaneous scheduling of MAC operations using RISC-V vector instructions, improving execution speed without adding extra hardware.

Function Inlining

Function inlining replaces a function call with the body of the function itself, eliminating call/return overhead. This is particularly useful for **small functions** common in embedded libraries, such as math routines, bit manipulation, or peripheral control functions.

Benefits:

- Eliminates stack operations and branching associated with function calls.
- Improves performance in real-time systems where frequent small function calls dominate execution time.
- Facilitates further compiler optimizations, such as constant propagation and loop vectorization.

Example:

- In a microcontroller controlling LED matrices, small functions to calculate pixel intensity are inlined, reducing execution time per update cycle by 12–15%.

4.3 Profile-Guided Optimization (PGO)

Profile-Guided Optimization leverages **runtime profiling information** to optimize code paths that are executed most frequently. In embedded workloads, certain loops or functions often dominate execution time, making PGO highly effective.

Workflow:

1. **Instrumentation Build:** The compiler inserts profiling instructions into the code.
2. **Execution Profiling:** The program runs on a representative dataset to collect execution statistics (e.g., frequently executed branches, loops, or functions).
3. **Optimized Rebuild:** The compiler uses the profiling data to reorder basic blocks, align frequently executed loops, and apply targeted inlining or unrolling.

Advantages for Embedded Systems:

- Optimizes hot paths for **performance-critical tasks**.

- Reduces **energy consumption** by minimizing unnecessary instruction execution.
- Improves **real-time predictability**, as heavily executed loops are better optimized.

Example:

- In a wearable fitness tracker, profiling revealed that the step-counting algorithm accounted for 60% of CPU time. Applying PGO allowed the compiler to inline key functions and unroll inner loops selectively, reducing execution time by 25% and energy per step-count computation by 18%.

5. HARDWARE-SOFTWARE CO-DESIGN APPROACHES

Optimizing RISC-V for embedded systems is most effective when hardware and software are designed together. Techniques include:

- **Custom accelerators for critical kernels:** e.g., MAC units for signal processing
- **Specialized memory hierarchies:** local scratchpad memory for fast access
- **ISA-aware compiler optimizations:** ensuring generated code utilizes hardware features efficiently

Table 2: Performance Improvement Using Co-Design Techniques

Optimization Technique	Latency Reduction	Energy Saving	Area Overhead
Compressed Instructions (RVC)	12%	15%	Low
Hardware Loop Support	20%	10%	Medium
Custom DSP Instructions	40%	25%	High
Vector Extensions (RVV)	50%	30%	High

6. CASE STUDIES IN EMBEDDED RISC-V OPTIMIZATION

6.1 IoT Sensor Node

- RISC-V core with RVC and custom MAC instructions
- Result: 35% reduction in execution time and 20% energy savings

6.2 Low-Power Audio Processing

- Vectorized filtering using RVV
- Compressed instructions for code-size optimization
- Result: 40% faster processing and 18% power reduction

6.3 Embedded ML Inference

- Custom instructions for matrix multiplication
- Hardware-software co-design approach
- Result: 3x speedup over baseline RISC-V implementation

7. CHALLENGES AND TRADE-OFFS

7.1 Hardware Complexity vs. Power

Adding custom instructions and accelerators increases silicon area and potentially static power. Designers must balance performance gains against area and leakage overhead.

7.2 Compiler Support

Many compiler optimizations require extensive profiling or manual tuning. Inconsistent support across toolchains can limit practical benefits.

7.3 Compatibility and Portability

Custom extensions improve performance but reduce portability across different RISC-V cores. Standardization efforts are needed to ensure software reusability.

7.4 Verification Complexity

Extended ISAs require more rigorous verification to ensure correctness, which can increase design time and cost.

8. FUTURE DIRECTIONS

1. **Standardized Custom Extensions for Embedded ML:** Shared libraries for DSP and ML accelerators.
2. **Dynamic ISA Adaptation:** Runtime selection of instruction sets based on workload characteristics.
3. **Energy-Aware Compiler Optimizations:** Adaptive compilation to optimize for energy or latency dynamically.
4. **Integration with Heterogeneous Cores:** Combining RISC-V cores with specialized accelerators for ultra-low power embedded systems.

9. CONCLUSION

RISC-V ISA optimization for embedded workloads provides a promising path toward high-performance, energy-efficient, and scalable systems. Compressed instructions, custom extensions, vector support, and co-design strategies collectively improve performance, reduce power consumption, and optimize memory usage. However, challenges related to hardware complexity, compiler support, and verification remain. Future research

should focus on standardized extensions for emerging embedded workloads, energy-aware compilation, and dynamic ISA adaptation. Optimizing RISC-V at multiple layers—hardware, ISA, compiler, and system—is key to meeting the increasingly demanding requirements of embedded applications.

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