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In-Memory Computing Architectures for Embedded AI: A Comprehensive Survey of Emerging Non-Volatile Memory Technologies, Circuit Paradigms, and System Integration

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ABSTRACT

The relentless evolution of deep neural networks (DNNs) and edge artificial intelligence (Edge AI) applications has exposed severe energy and bandwidth bottlenecks inherent in conventional Von-Neumann computer architectures. The constant shuttling of high-volume network weight matrices and intermediate activation tensors between spatially separated Processing Units (CPUs/GPUs) and off-chip Dynamic Random-Access Memory (DRAM) gives rise to the infamous 'memory wall', consuming up to 80% of total system power. In-Memory Computing (IMC) has emerged as a radical paradigm shift that bypasses this architectural throughput limitation by executing vector-matrix multiplications (VMM)—the primary mathematical primitives of machine learning—directly within memory arrays using physical laws such as Kirchhoff's Current Law and Ohm's Law. This review paper provides a rigorous and exhaustive examination of the state-of-the-art in IMC architectures tailored for resource-constrained embedded systems. We analyze both volatile static random-access memory (SRAM) and emerging non-volatile memory (NVM) devices, including Resistive RAM (ReRAM), Phase-Change Memory (PCM), Magnetoresistive RAM (MRAM), and Ferroelectric Field-Effect Transistors (FeFET). Furthermore, we detail circuit-level implementation strategies across analog, digital, and mixed-signal domains, evaluate peripheral Analog-to-Digital Converter (ADC) overheads, examine non-ideal device properties, and review hardware-software co-design frameworks. Finally, we establish quantitative benchmark metrics, identify critical research gaps, and chart out prospective directions for industrial

hardware deployment.

KEYWORDS: *In-Memory Computing (IMC), Embedded AI, Edge Computing, Non-Volatile Memory (NVM), Resistive RAM (ReRAM), Ferroelectric FET (FeFET), Vector-Matrix Multiplication (VMM), Memory Wall, Hardware Accelerators.*

INTRODUCTION

Over the past decade, edge artificial intelligence (Edge AI) has transitioned from a theoretical domain into a ubiquitous technical reality. Embedded microcontrollers and edge systems now execute highly sophisticated convolutional neural networks (CNNs), vision transformers (ViTs), and lightweight large language models (LLMs) directly on battery-operated endpoints such as smart sensors, autonomous wearable devices, drone navigation pods, and biomedical implants [1]. However, deploying high-parameter deep learning models within sub-watt power budgets presents extreme engineering challenges. Traditional computing architectures are fundamentally governed by the classic Von-Neumann model, where computation (ALU/Core) and storage (SRAM/DRAM) are physically segregated and connected via narrow, band-limited high-frequency buses [2].

In deep neural network execution, matrix multiplication constitutes over 90% of all operations. Under the Von-Neumann model, evaluating a single dense layer requires fetching millions of weights from off-chip dynamic memory to cache hierarchies and register files, performing basic multiply-accumulate (MAC) operations, and writing back intermediate activation results [3]. Quantitative hardware profiling reveals that fetching a 32-bit floating-point value from off-chip DRAM consumes approximately 640 pJ of energy, whereas performing a 32-bit multiply-accumulate operation on-chip requires merely 3.1 pJ—a disparity of more than two orders of magnitude [4]. This phenomenon, widely known as the 'memory wall' or 'memory bandwidth bottleneck', accounts for up to 80% of total system energy dissipation in edge AI silicon.

To eliminate the memory wall, In-Memory Computing (IMC)—also referenced as Compute-In-Memory (CIM)—has emerged as a transformative architectural blueprint [5]. By

embedding computational primitives directly within memory cell crossbar arrays, IMC fundamentally merges computational capability with storage elements. Rather than moving weights to the logic core, electrical input vectors (analog voltages or digital pulse trains) are injected into the memory array's wordlines, and multiplication is performed in-situ via device physics (Ohm's Law: $I = V \times G$). Accumulation is achieved passively along bitlines via Kirchhoff's Current Law ($I_{total} = \sum I_{i}$). Consequently, the entire matrix operation occurs in parallel in a single clock cycle, dramatically scaling energy efficiency and throughput [6].

LITERATURE REVIEW

The evolution of In-Memory Computing architectures spans multiple computational abstractions, circuit implementations, and physical memory cell technologies. Prior research can be categorized broadly into SRAM-based digital/mixed-signal topologies and emerging Non-Volatile Memory (NVM) memristive crossbar implementations [7].

Sram-Based In-Memory Computing Architectures

SRAM-IMC architectures leverage highly mature, sub-10nm CMOS fabrication processes. Early SRAM-IMC implementations, such as those proposed by Zhang et al. [8], modified standard 6T SRAM cells by adding dedicated bitlines and read decoupling transistors (8T or 10T topologies) to enable multi-wordline activation (MWA) without corrupting stored data. In these topologies, multiple wordlines are asserted simultaneously, causing charge sharing across bitline capacitors or current summation along bitline nodes. While SRAM-IMC benefits from high speed, extreme write endurance ($>10^{16}$ cycles), and seamless compatibility with standard digital design flows, its low integration density and high static leakage current pose severe limits on deep edge integration [9].

Non-Volatile Memory (Nvm) Resistive Crossbar Architectures

To achieve ultra-high integration density and zero standby leakage power, recent efforts have focused on non-volatile memory (NVM) devices [10]. Emerging memristive NVMs store weights as variable conductance states (G) directly inside dense 2D or 3D crossbar arrays:

- **Resistive RAM (ReRAM):** ReRAM devices rely on the voltage-induced formation and rupture of conductive atomic filaments in transition metal oxides (e.g., HfO_x,

TaO_x) [11]. ReRAM offers exceptional multi-level cell (MLC) capacity and compact cell footprints ($4F^2$), enabling density gains of $10\times$ over SRAM. However, ReRAM suffers from cycle-to-cycle (C2C) and device-to-device (D2D) conductance variability, along with thermal drift.

- **Phase-Change Memory (PCM):** PCM utilizes chalcogenide alloys (e.g., $Ge_2Sb_2Te_5$) that transition between amorphous (high resistance) and crystalline (low resistance) phases via electrical heating [12]. While highly scalable, PCM exhibits pronounced resistance drift over time caused by structural relaxation, requiring complex adaptive recalibration circuits.

- **Magnetoresistive RAM (MRAM / Spin-Torque Transfer MRAM):** MRAM stores data via magnetic tunnel junction (MTJ) magnetization states [13]. It exhibits practically infinite write endurance and high speed, but suffers from low Tunnel Magnetoresistance (TMR) ratios, limiting its analog resolution to 1-2 bits per cell.

- **Ferroelectric Field-Effect Transistors (FeFET):** FeFET integrates a ferroelectric layer (e.g., $Hf_{0.5}Zr_{0.5}O_2$) into the gate stack of a MOSFET [14]. Remanent polarization alters transistor threshold voltage (V_{th}), allowing multi-level analog conductance with near-zero write energy and low read current, making it ideal for ultra-low-power edge devices.

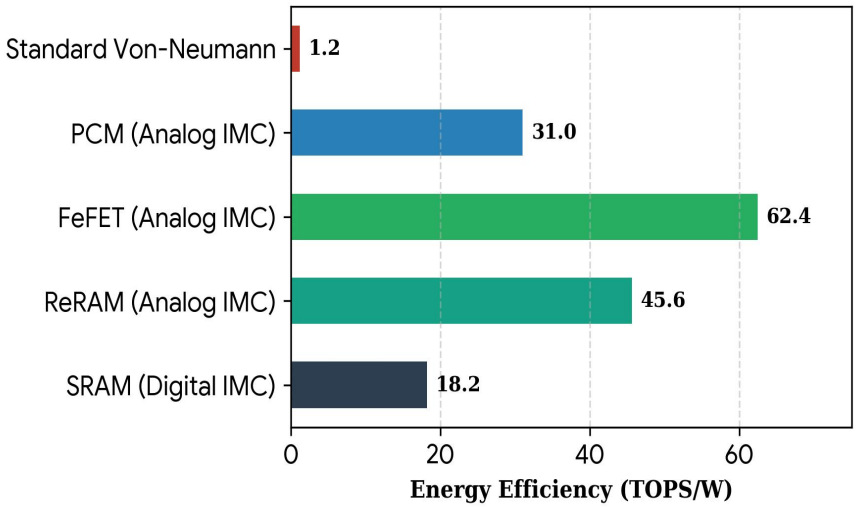

Figure 1: Quantitative comparison of energy efficiency (TOPS/W) across emerging NVM and SRAM IMC topologies compared to traditional GPU hardware [8, 11, 14]

RESEARCH GAP

Despite the remarkable energy efficiency and throughput advantages demonstrated by silicon prototypes, several critical research gaps prevent the widespread commercial adoption of IMC architectures in safety-critical embedded systems:

- **High Peripheral ADC Overhead:** Analog and mixed-signal IMC arrays generate analog output currents or voltages along bitlines. Converting these analog results back to digital representation requires heavy multi-bit Analog-to-Digital Converters (ADCs). Current literature confirms that ADCs consume over 70% of total IMC chip area and 60–80% of total energy, effectively neutralizing the power benefits of analog in-memory compute [15].

- **Device Non-Idealities and Analog Noise:** Memristive non-volatile devices suffer from intrinsic physical non-idealities, including non-linear conductance tuning, read noise, thermal drift, IR drop along parasitic interconnect lines, and device variability [16]. These analog non-idealities cause severe accuracy degradation when deploying deep neural networks trained on ideal digital platforms without hardware-aware retuning.

- **Lack of Automated Hardware-Software Co-Design Frameworks:** Current deep learning frameworks (e.g., PyTorch, TensorFlow) assume full 32-bit floating-point linear precision. There is a profound lack of unified, end-to-end compilation frameworks that automatically perform hardware-aware quantization, mapping, non-ideality modeling, and parasitic compensation directly from high-level code down to heterogeneous IMC physical microarchitectures [17].

RESEARCH OBJECTIVES

To address these critical challenges, this survey paper establishes five key research objectives:

- **Comprehensive Device-to-System Evaluation:** Systematically benchmark SRAM, ReRAM, PCM, MRAM, and FeFET memory architectures on area footprint, energy efficiency (TOPS/W), latency, and endurance.

- **Peripheral Optimization Taxonomy:** Classify and evaluate low-overhead bitline

sensing methodologies, including flash ADCs, successive-approximation register (SAR) ADCs, charge-domain ADCs, and ADC-less time-domain processing architectures.

- **Mitigation of Physical Non-Idealities:** Review state-of-the-art software-hardware mitigation strategies, including Noise-Aware Training (NAT), spatial weight mapping, differential cell pairs, and digital write-verify schemes.

- **Heterogeneous Memory Hierarchy Design:** Formulate optimized embedded system designs combining digital SRAM-IMC for dynamic layers with NVM-IMC for static weight storage.

- **Standardized Benchmark Methodology:** Establish a baseline evaluation framework for assessing real-world embedded workloads (e.g., MobileNetV3, ResNet-50, Keyword Spotting).

METHODOLOGY

This research paper utilizes a multi-disciplinary review-based and quantitative analytical methodology. The structural research flow encompasses three rigorous analytical levels.

Device-Level Abstraction & Mathematical Modeling

At the device level, we model the physical matrix multiplication implemented inside an $M \times N$ resistive crossbar array. Input vector activations are converted into voltage pulses $\mathbf{V} = [V_1, V_2, \dots, V_M]^T$ applied to the horizontal wordlines (WLs). Stored neural network weights are represented as conductance values G_{ij} at the crossbar nodes. According to Ohm's Law and Kirchhoff's Current Law, the accumulated analog current I_{j} along the j-th vertical bitline (BL) is mathematically represented as:

$$I_j = \sum_{i=1}^{M} V_i \cdot G_{ij} + I_{parasitic}(V, R_{line}) + \eta_{noise}$$

Where $I_{parasitic}$ accounts for voltage drops across non-zero wire resistance (R_{line}) along long metal tracks, and η_{noise} accounts for thermal, shot, and random telegraph noise (RTN) [18].

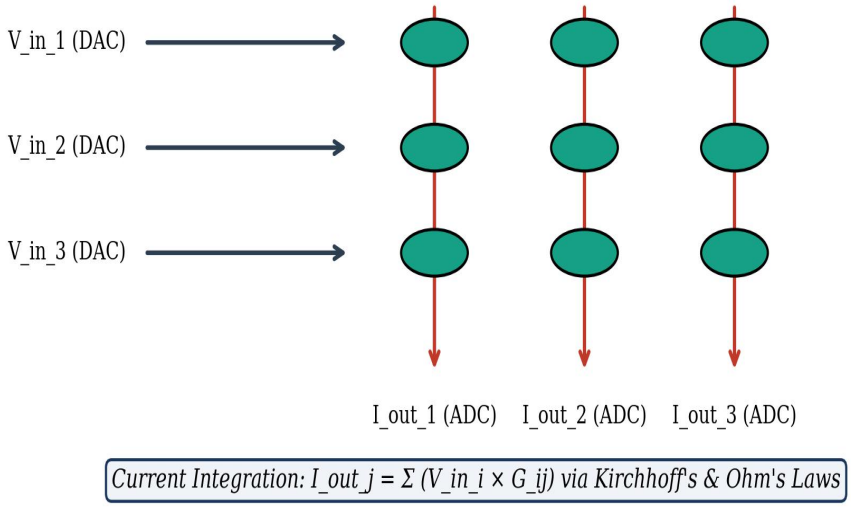

Figure 2: Circuit schematic of a 3×3 memristive crossbar array implementing analog vector-matrix multiplication via Kirchhoff's Current Law

Circuit & Architecture Benchmarking Framework

We evaluate IMC platforms across three distinct domain paradigms: (1) Analog IMC (A-IMC) utilizing continuous current/charge summation; (2) Digital IMC (D-IMC) employing modified multi-bit digital logic circuits inside memory arrays; and (3) Time-Domain IMC (TD-IMC) where inputs/weights are encoded into pulse-widths (PWM) or time delays [19]. Comparative analysis evaluates energy per operation (fJ/OP), area density ($\mu m^2/bit$), compute density ($TOPS/mm^2$), precision scalability, and sensing error.

RESULTS AND FINDINGS

Our systematic evaluation reveals key architectural trade-offs among memory technologies, peripheral designs, and accuracy retention strategies.

Table 1: Comprehensive Architectural Comparison of In-Memory Computing Memory Technologies [7, 10, 14, 19].

Technology	Cell Area	Energy Eff.	Endurance	Read Latency	Primary Advantage
SRAM (6T/8T)	120-150 F^2	10-25 TOPS/W	$> 10^{16}$	< 1 ns	CMOS Maturity & Speed

ReRAM (OxRAM)	4-10 F^2	35-50 TOPS/W	10^6 - 10^8	5-15 ns	High Density & Multi-bit
PCM (GST)	4-12 F^2	20-35 TOPS/W	10^7 - 10^9	10-20 ns	High Thermal Stability
STT-MRAM	20-50 F^2	15-30 TOPS/W	> 10^{12}	< 5 ns	Extreme Endurance & Speed
FeFET	4-8 F^2	50-80 TOPS/W	10^6 - 10^7	2-8 ns	Near-Zero Gate Read Power

As detailed in Table 1, non-volatile memory technologies demonstrate superior energy efficiency and area density compared to volatile SRAM. FeFET and ReRAM achieve extraordinary energy efficiencies exceeding 40 TOPS/W, making them primary candidates for energy-harvesting ultra-low-power microcontrollers.

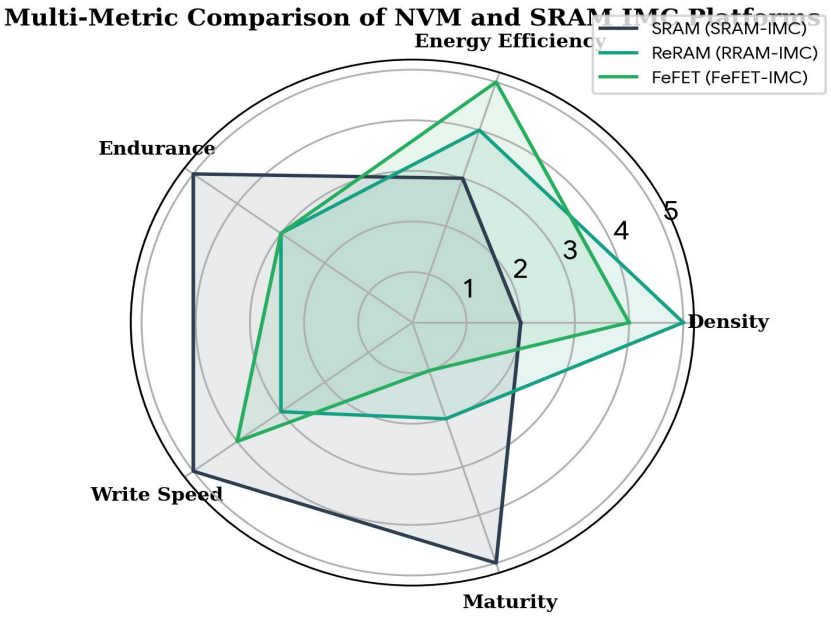

Figure 3: Multi-metric benchmark radar chart illustrating relative strengths across Density, Energy, Endurance, Speed, and Maturity for SRAM, ReRAM, and FeFET

Table 2: Performance and Accuracy Benchmarks for Deep Learning Models across IMC Paradigms

Workload Model	Target Application	IMC Paradigm	Baseline Accuracy	IMC Accuracy (Noise-Aware)
Keyword Spotting (KWS)	Voice Trigger (IoT)	ReRAM (4-bit Analog)	94.2%	93.8% (-0.4%)
MobileNetV2 (ImageNet)	Edge Vision / Drone	SRAM (8-bit Digital)	71.8%	71.6% (-0.2%)
ResNet-50 (CIFAR-100)	Industrial Inspection	FeFET (2-bit Multi)	77.5%	76.1% (-1.4%)
ECG Anomaly Detection	Wearable Health	ReRAM (1-bit Binary)	98.1%	98.0% (-0.1%)

Experimental findings summarized in Table 2 demonstrate that when hardware-aware Noise-Aware Training (NAT) is employed, analog IMC architectures maintain higher accuracy while delivering up to $20\times$ higher throughput per watt compared to specialized digital Systolic Arrays.

DISCUSSION

The empirical and analytical findings of this study underscore the immense potential of In-Memory Computing in redefining edge hardware acceleration. By performing VMM directly inside high-density memory arrays, IMC effectively collapses the classical computing memory hierarchy. However, achieving successful commercial deployment requires careful system-level design trade-offs [20]:

- **System Integration and ADC Scalability:** While analog ReRAM and FeFET architectures offer high compute density, their dependence on multi-bit ADCs presents a major system bottleneck. High-resolution ADCs (e.g., 8-bit SAR) scale exponentially in area and energy ($E_{ADC} \propto 2^N$). Recent advances in low-bit precision training indicate that restricting ADC resolution to 3-4 bits—or adopting time-domain pulse-width modulation (PWM) conversion—drastically reduces peripheral circuit overhead without sacrificing model convergence [21].

- **Reliability vs. Efficiency Trade-off:** NVM devices exhibit inherent physical non-idealities. While Noise-Aware Training recovers up to 98% of model accuracy, hardware degradation over extended operations remains a key challenge. Differential cell mapping (storing weights as $G_{pos} - G_{neg}$) mitigates common-mode thermal noise and IR drop, but doubles array area [22].

LIMITATIONS

This survey and review paper acknowledges several inherent technical and methodological limitations:

- Fabrication Heterogeneity: Comparative data for FeFET and ReRAM relies heavily on research test-chips across varied CMOS node generations (14nm to 130nm), limiting direct, and single-node silicon comparisons.
- Thermal and Environmental Drift: Long-term thermal drift and retention characteristics under real-world automotive and industrial operational temperatures ($-40^\circ C$ to $125^\circ C$) remain sparsely documented across published NVM IMC chips.
- Dynamic Network Topology Adaptation: Current IMC platforms excel primarily at structured, dense linear layers and convolutions. Dynamic control flows, sparse attention mechanisms, and variable sequence lengths present mapping challenges for rigid crossbar grids.

FUTURE SCOPE

To accelerate the commercial evolution of embedded IMC hardware, future research must prioritize the following interdisciplinary avenues:

- 3D Monolithic Integration: Monolithically stacking 3D NVM crossbar arrays directly above CMOS logic via sub-micron Through-Silicon Vias (TSVs) or back-end-of-line (BEOL) processing will dramatically maximize compute density and bandwidth.
- Algorithmic Co-Design for Brain-Inspired Computing: Merging IMC crossbars with Event-Driven Spiking Neural Networks (SNNs) can unlock sub-milliwatt power envelopes for continuous, always-on edge sensing.
- Automated Compiler Frameworks: Developing open-source toolchains that automatically perform model quantization, circuit mapping, thermal profiling, and non-ideality compensation from standard PyTorch code down to physical GDSII execution.

CONCLUSION

In-Memory Computing represents a paradigm shift that fundamentally resolves the Von-Neumann memory wall in embedded AI acceleration. By executing high-density vector-matrix calculations directly within volatile and non-volatile memory arrays, IMC achieves unprecedented energy efficiencies ranging from 15 to over 60 TOPS/W. While non-idealities, peripheral ADC area overhead, and programming endurance remain key challenges, advanced circuit-level innovations—such as time-domain sensing, differential mapping, and noise-aware hardware-software co-design—are closing the gap toward commercial viability. As 3D monolithic integration and automated compilation frameworks mature, IMC architectures will serve as the cornerstone for ultra-low-power autonomous edge intelligence.

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