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Voltage Regulation Assessment of a D-STATCOM on the IEEE 13-Bus Feeder

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ABSTRACT

Voltage sag along radial medium-voltage distribution feeders worsens as load grows, and utilities increasingly rely on Distribution Static Synchronous Compensators (D-STATCOMs) for fast, continuously adjustable reactive power support. However, many published D-STATCOM studies compare a compensated feeder only against an uncompensated one, without directly contrasting the STATCOM's dynamic behavior against a conventional fixed capacitor of the same MVAr rating. This study models the IEEE 13-Node Distribution Test Feeder as a balanced positive-sequence equivalent, solved with the backward/forward sweep load-flow method, and compares three reactive power compensation strategies — no compensation, a fixed capacitor, and a droop-controlled D-STATCOM, both rated at 1.5 MVAr — across ten feeder loading levels (10–100% of rated load, in 10% steps) at all eight of the feeder's load-carrying buses. Results show the two devices perform identically once loading exceeds their shared rating, but below that point their behavior diverges sharply: at 10% load, the fixed capacitor overvoltages the bus to 1.0333 pu and, counter-intuitively, increases total feeder real-power loss more than fifteen-fold above the uncompensated case (18.575 kW vs. 1.150 kW, concentrated in the trunk branches carrying the excess reactive current), whereas the D-STATCOM holds the bus at exactly 1.0000 pu while keeping losses at or below the uncompensated baseline at every loading level tested. A full siting sweep across all eight load buses shows both the loss-reduction benefit and the crossover load level are site-dependent: Bus 671, the feeder's main junction, achieves the largest loss reduction (28.3%) and the earliest crossover (60% load), while Bus 634, isolated behind the feeder's step-down transformer, achieves only 1.7% loss reduction and never saturates its 1.5 MVAr rating even at full load. The

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uncompensated worst-case sag of 0.9178 pu is consistent with sag magnitudes (0.9081–0.9131 pu) reported for real Indian distribution feeders in prior studies. An independent Newton-Raphson implementation reproduced all backward/forward sweep results to within 5×10^{-5} pu, cross-validating the solver implementation itself (though not the balanced-equivalent modeling assumption against the feeder's official unbalanced specification).

KEYWORDS: *D-STATCOM; voltage regulation; reactive power compensation; IEEE 13-bus feeder; power loss; backward/forward sweep*

INTRODUCTION

Radial medium-voltage (MV) distribution feeders experience a progressive voltage drop from the substation toward the end of the feeder, and this sag deepens as connected load grows — a persistent operational problem for distribution utilities, particularly on long rural feeders with high R/X ratios. Reactive power compensation is the standard remedy, and among the available technologies, the Distribution Static Synchronous Compensator (D-STATCOM) has drawn sustained research interest because, unlike a fixed or mechanically switched capacitor bank, its power-electronic converter can continuously modulate its reactive output in response to the network condition [1], [8]. Early MATLAB/Simulink-based investigations established this modulation capability on test power systems, demonstrating the STATCOM's effect on system voltage stabilization and power factor correction [10]. Recent work continues to explore D-STATCOM integration alongside distributed photovoltaic generation to jointly manage voltage and cost in modern distribution networks [5], [7], reflecting the device's growing relevance as feeders absorb more variable load and generation.

Prior studies, surveyed comprehensively in recent review literature covering sizing, control, and renewable integration [12], have approached D-STATCOM performance mainly from two directions. One line of work develops metaheuristic algorithms to determine optimal D-STATCOM location and size on standard or real distribution feeders, reporting loss reduction and voltage-profile improvement relative to an uncompensated base case [4], [6], including time-varying, multi-unit placement studies using particle swarm optimization [11]. A second line of work, exemplified by Dash, Mishra, and Abdelaziz [3], develops improved D-STATCOM load-flow models and validates them on both a standard 33-bus system and a

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practical 51-bus rural Indian distribution feeder, reporting a base-case minimum voltage of 0.9081 pu without compensation, and further performs an economic comparison of the number of D-STATCOM units to deploy. Similarly, Mossie et al. [6] validate a joint STATCOM/DG placement method on real feeders in Bahir Dar, Ethiopia. What is comparatively less examined in this literature is a direct, controlled comparison between a D-STATCOM and a conventional fixed capacitor of identical MVAr rating across a fine-grained range of loading conditions and more than one installation site on a single, widely recognized benchmark feeder — most studies instead compare a compensated case only against an uncompensated one, or compare different optimization algorithms against each other at a single, pre-optimized site, which does not isolate the specific loading range and location dependence of the STATCOM's advantage over static compensation.

This study addresses that gap by modeling the IEEE 13-Node Test Feeder [1], a standard, publicly specified benchmark distribution network, as a balanced positive-sequence equivalent, and comparing three reactive power compensation strategies — no compensation, a fixed capacitor, and a droop-controlled D-STATCOM, with the capacitor and STATCOM given the same MVAr rating — across ten loading levels from 10% to 100% of rated load at every one of the feeder's eight load-carrying bus locations. The objective is to (i) quantify, for an equally sized device pair, the specific loading range over which the STATCOM's dynamic modulation yields a measurable voltage and loss advantage over static compensation; (ii) determine how that loading range and the magnitude of the loss-reduction benefit vary with the compensation site across the whole feeder; and (iii) benchmark the resulting sag magnitudes against previously published results from real Indian and Ethiopian distribution feeders [3], [6].

RESEARCH METHODS

1. Test Feeder and Modeling Approach

The IEEE 13-Node Test Feeder [1] is a short, heavily loaded, officially specified radial MV feeder widely used to benchmark distribution analysis software. Its official specification is unbalanced three-phase, with a substation voltage regulator, an in-line step-down transformer, and mixed overhead/underground line segments. For tractability with a single-phase backward/forward sweep solver, this study uses a balanced positive-sequence equivalent: the topology, branch lengths, and total (summed three-phase) real/reactive load at

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each bus are taken directly from the official specification [1]; branch resistance is taken from the official conductor resistance table; branch reactance is computed from the official conductor GMR values using the standard single-frequency inductive reactance formula with a representative phase spacing.

The substation voltage regulator and the original fixed capacitor banks specified in [1] are deliberately excluded from the base case. This is a controlled methodological choice, not an oversight: the objective of this study is to isolate the differential behavior between two compensation devices under otherwise identical conditions, and retaining the original regulator/capacitor scheme would introduce a confounding, pre-existing compensation layer that masks the comparison the study is designed to make. The resulting simplification means the uncompensated "no compensation" case is a deliberately worst-case, unregulated feeder, not a claim about how the real IEEE 13-node feeder performs in its official configuration; this is stated explicitly as a limitation in Section 3.7, and reproducing this comparison with the full unbalanced, regulator-equipped feeder in dedicated distribution analysis software is identified as priority future work.

2. Backward/Forward Sweep Load Flow

Because the feeder is radial (tree-structured, no loops), the network is solved with the backward/forward sweep method, the standard approach for distribution system load flow given the high R/X ratios typical of MV/LV feeders [2].

For each node n with children c(n), the backward sweep computes the current drawn toward the source:

$$I_n = \mathrm{conj}(S_n / V_n) + \Sigma\, I_c \quad \text{for all children } c \text{ of } n$$

and the forward sweep updates each child bus voltage from its parent:

$$V_c = V_{\mathrm{parent}(c)} - Z_{(\mathrm{parent}(c),c)} \cdot I_c$$

where $S_n = P_n + jQ_n$ is the complex load at bus n and Z is the branch impedance. The two sweeps repeat until the largest voltage change between successive iterations falls below 1×10^{-9} pu. Total feeder power loss is then computed as the sum, over every branch, of the branch current magnitude squared times the branch impedance:

$$S_{loss} = \Sigma\, |I_{branch}|^2 \cdot Z_{branch} = P_{loss} + jQ_{loss}$$

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3. Compensation Device Models

Three cases are solved at the compensation bus for each loading level, repeated at every one of the feeder's eight load-carrying bus locations (Section 3.3):

- No compensation — the baseline radial load flow with no shunt device.
- Fixed capacitor — a constant reactive injection equal to the device's full rating Q_max, regardless of loading.
- D-STATCOM — a controllable reactive source at the same bus, updated after each load-flow solution by a proportional-integral droop law:

  $Q_c \leftarrow clamp(\ Q_c + K\cdot(V_set - |V_bus|),\ -Q_max,\ +Q_max\ )$

with control gain K = 1.5 and Q_max = 1.50 MVAr for both devices, giving a like-for-like comparison of identically rated hardware under two different control philosophies. Figure 1 summarizes the full solution procedure.

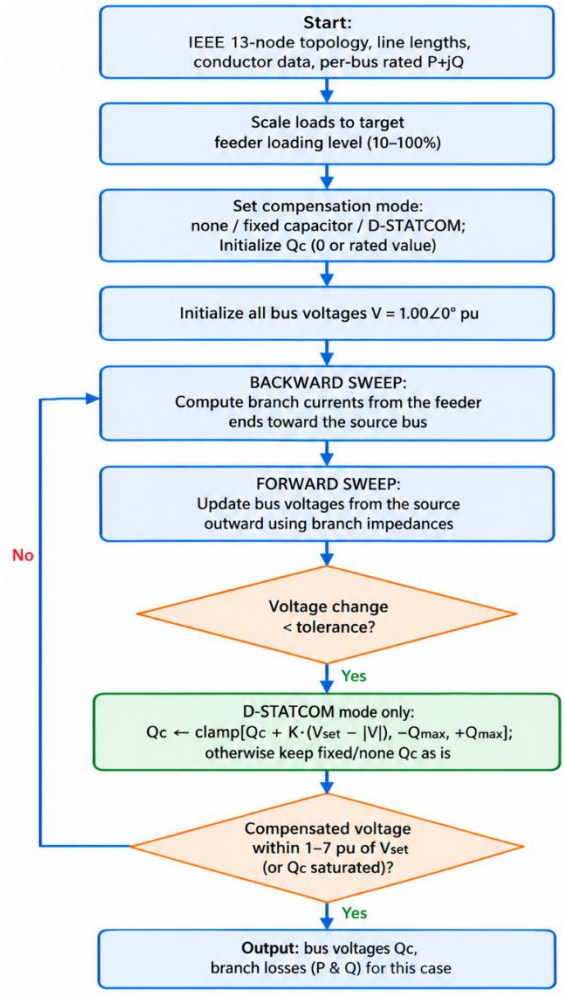


Figure 1: Flowchart of the backward/forward sweep load flow with the D-STATCOMdroop-control outer loop.

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4. Loading and Siting Scenarios

All bus loads are scaled uniformly from 10% to 100% of the rated values in Table 1, in 10% steps, giving 10 loading levels × 3 compensation strategies × 8 compensation sites (every load-carrying bus on the feeder) = 240 simulation cases in total.

Table: 1

Parameter	Symbol	Value
Base power	S_base	1 MVA
Nominal feeder voltage	V_base	4.16 kV
Test feeder	—	IEEE 13-Node Test Feeder [1]
Total connected load	∑P, ∑Q	3.466 MW, 2.102 MVAr
Number of buses / branches	—	13 buses / 12 branches
Primary illustrative bus	—	Bus 675
Full siting sweep	—	All 8 load-carrying buses
Voltage setpoint (D-STATCOM)	V_set	1.00 pu
Device MVAr rating (both cases)	Q_max	1.50 MVAr
Loading levels simulated	—	10-100% of rated, 10% steps
Slack (substation) bus voltage	V_{650}	1.00 ∠ 0° pu

RESULTS AND DISCUSSION

1. Bus Voltage Across Loading Levels

Table 2 summarizes representative results at Bus 675; Figure 2 shows the full 10-point sweep.

Table: 2

Load (%)	Compensation	Qc (MVAr)	V_{675} (pu)	P loss (kW)	vs. none
10	None	0.000	0.9925	1.150	—
10	Fixed capacitor	1.500	1.0333	18.575	+1515%

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10	D-STATCOM	0.265	1.0000	1.035	−10%
50	None	0.000	0.9612	30.517	—
50	Fixed capacitor	1.500	1.0040	28.350	−7%
50	D-STATCOM	1.354	1.0000	26.487	−13%
60	None	0.000	0.9529	44.653	—
60	Fixed capacitor	1.500	0.9963	36.741	−18%
60	D-STATCOM (saturates here)	1.500	0.9963	36.741	−18%
100	None	0.000	0.9178	132.953	—
100	Fixed capacitor	1.500	0.9640	97.562	−27%
100	D-STATCOM (saturated)	1.500	0.9640	97.562	−27%

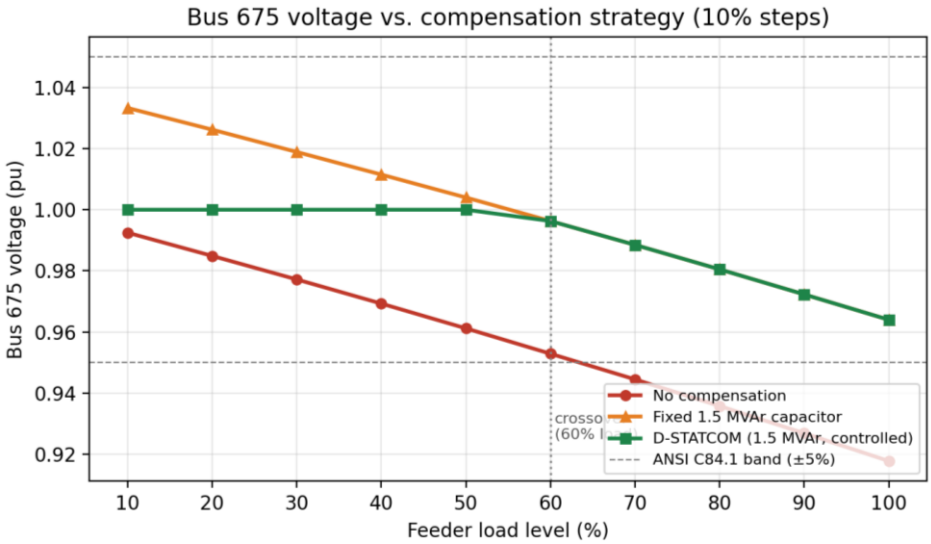


Figure 2: Bus 675 Voltage vs. Feeder Loading for the Three Compensation Strategies, Against the ANSI C84.1 ±5% Service Voltage Band [9].

Without compensation, Bus 675 voltage falls from 0.9925 pu at 10% load to 0.9178 pu at 100% load. Both compensation devices restore acceptable voltage at full load (0.9640 pu), but their behavior diverges sharply at light load: the fixed 1.5 MVAr capacitor, unable to

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reduce its output as load falls, overcompensates and pushes the bus to 1.0333 pu at 10% load, while the D-STATCOM — injecting only the 0.265 MVAr actually required — holds the bus at exactly the 1.00 pu setpoint at every loading level up to the crossover point.

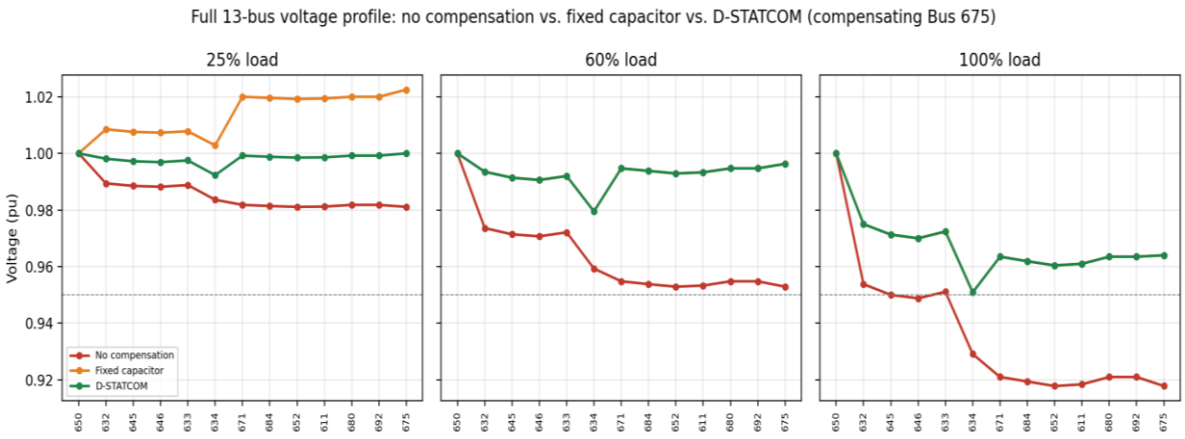


Figure 2b: Full 13-Bus Voltage Profile (All Buses, Not Only The Compensated Bus) At 25%, 60%, And 100% Load.

Figure 2b extends this beyond the single compensated bus: the fixed capacitor's light-load overvoltage and the D-STATCOM's exact 1.00 pu regulation are visible across the entire downstream feeder (buses 671 through 675), not only at the directly compensated bus, confirming the compensation effect propagates through the network rather than being a local artifact.

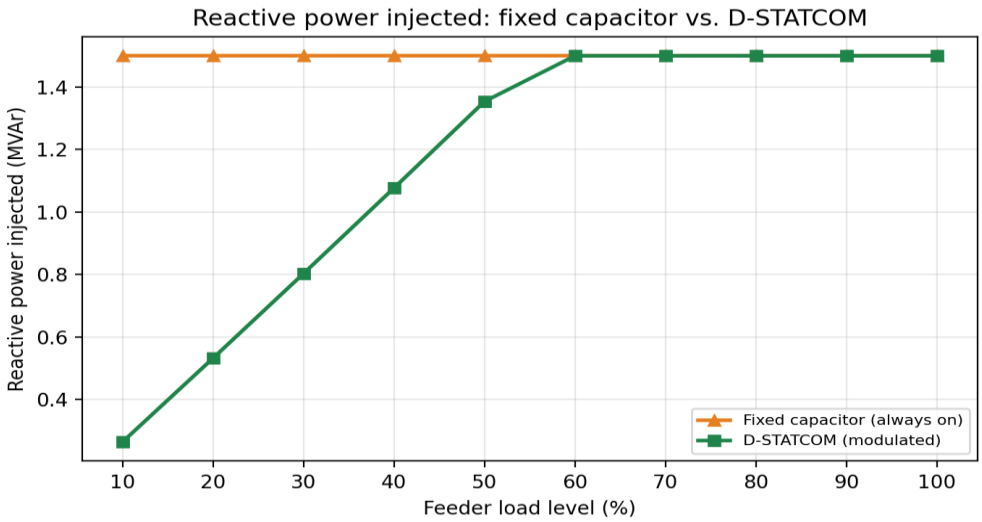


Figure 3: Reactive power injected by the fixed capacitor (constant) vs. the D-STATCOM (load-following) across the full loading sweep.

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2. Power Loss Results

Figure 4 reports total feeder real-power loss for all three strategies. This result is, in the author's assessment, the strongest finding of this study: at light loading (10–40%), the fixed capacitor does not merely fail to help — it makes feeder losses substantially worse than doing nothing. At 10% load, the fixed capacitor's forced 1.5 MVAr injection, far in excess of the 0.265 MVAr the feeder actually needs, drives large reactive circulating current through the feeder's branches, raising real power loss to 18.575 kW versus only 1.150 kW with no compensation at all — a more than fifteen-fold increase. The D-STATCOM, by injecting only what is needed, keeps losses at or below the uncompensated baseline across the entire loading range tested (10–100%), and its advantage over the fixed capacitor grows to roughly 27% loss reduction at full load.

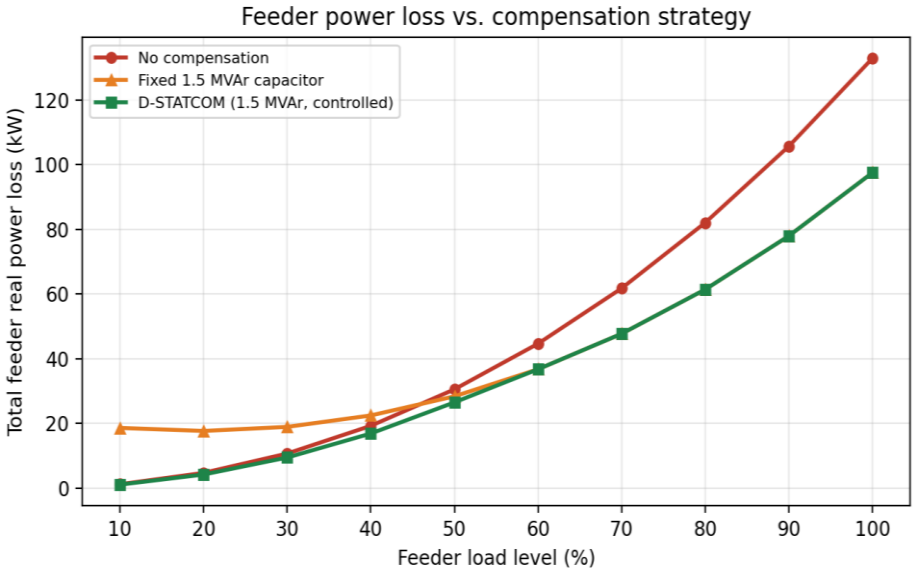


Figure 4: Total Feeder Real Power Loss vs. Compensation Strategy Across The Loading Sweep.

Branch-Level Loss Breakdown

To identify which parts of the feeder drive the loss increase in Section 3.2, per-branch losses were computed directly from the load-flow branch currents ($P_{loss,branch} = |I_{branch}|^2 \cdot R_{branch}$) at 10% load, comparing no compensation against the fixed capacitor.

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Table: 3

Branch	No comp. (kW)	Fixed cap. (kW)	Δ (kW)	% incr.
632-671	0.3644	7.2041	+6.8397	+1877%
650-632	0.6778	6.8077	+6.1299	+904%
692-675	0.0210	4.4562	+4.4352	+21120%
671-692	0.0002	0.0239	+0.0237	+11850%

(Remaining eight branches, all outside the 671–675 path, show losses within ±0.002 kW of the uncompensated case — a negligible second-order effect from the small voltage change at Bus 671.)

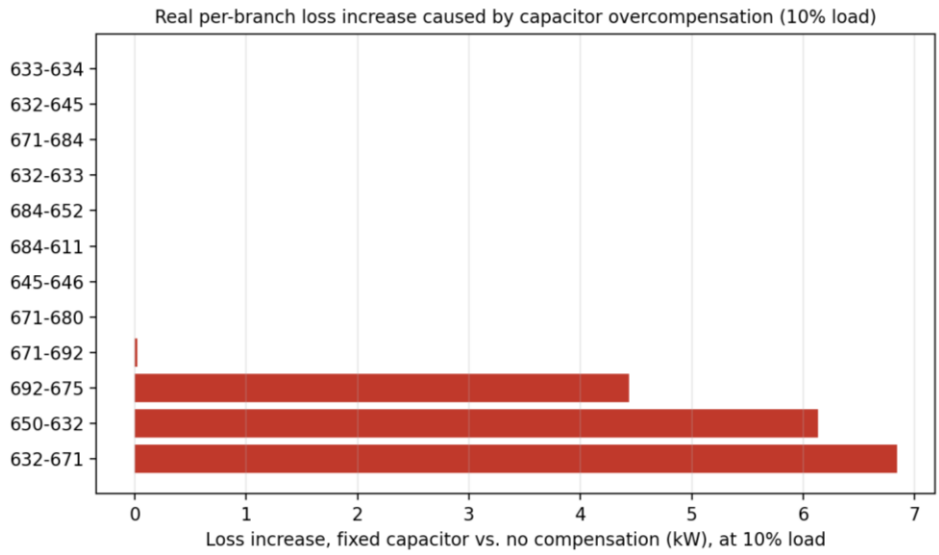


Figure 4b: Real Per-Branch Loss Increase from Capacitor Overcompensation At 10% Load.

The loss increase concentrates almost entirely on the two trunk segments carrying current from the substation to the compensation point (650-632 and 632-671) and the short segment feeding Bus 675 directly (692-675). This is physically consistent: the capacitor's forced 1.5 MVAr injection, far exceeding the 0.265 MVAr actually needed at 10% load, creates a large reactive current that must flow through these specific trunk branches, and I^2R loss scales with the square of that excess current.

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3. Compensation-Site Sensitivity

To test whether the crossover behavior above is specific to Bus 675, the D-STATCOM was relocated in turn to every one of the feeder's eight load-carrying buses, and the same 10–100% loading sweep was repeated at each site. Table 4 reports, for each site: the unconstrained reactive power that would be needed to hold 1.00 pu at 100% load; whether the 1.5 MVAr device saturates at 100% load; the resulting minimum feeder-wide voltage; the real-power loss reduction relative to no compensation; and the crossover load level (thefirst 10%-step loading level at which the device saturates).

Table: 4

Bus	Qreq (MVAr, unconstr.)	Saturated @100%	V_{min} (pu)	Loss reduction	Crossover (%)
671	2.899	Yes	0.9509	28.28%	60
692	2.899	Yes	0.9509	28.28%	60
645	2.785	Yes	0.9392	11.56%	60
675	2.785	Yes	0.9509	26.62%	60
611	2.512	Yes	0.9507	16.51%	70
646	2.496	Yes	0.9391	6.05%	70
652	2.447	Yes	0.9506	8.47%	70
634	1.216	No	0.9348	1.73%	none (never saturates)

This sweep reveals that Bus 671 — the feeder's main junction, not Bus 675 originally selected for illustration in Sections 3.1–3.2 — gives the best loss reduction (28.28% vs. 26.62% at Bus 675), because it sits upstream of more of the feeder's downstream load, so compensating there benefits a larger share of the network's branches. Bus 634, behind the feeder's step-down transformer, is the clear worst site: its 1.5 MVAr device never saturates even at 100% load, but it also achieves only a 1.73% loss reduction, because the transformer impedance largely decouples it from the rest of the feeder. The crossover load level itself clusters into two groups — 60% for buses electrically close to the main trunk (671, 692, 645, 675) and 70% for buses further out on laterals (611, 646, 652) — indicating that both the magnitude of a D-STATCOM's benefit and the load level at which that benefit disappears are

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governed by electrical proximity to the feeder's main power flow, not simply by the bus's own load size.

4. Comparison with Previously Published Feeders

Table: 5

Source	Feeder	Min. voltage (no comp.)
This study	IEEE 13-bus (positive-seq. equiv.)	0.9178 pu
Dash, Mishra&Abdelaziz [3]	Practical 51-bus rural feeder, India	0.9081 pu
Dash, Mishra&Abdelaziz [3]	Standard 33-bus system	0.9131 pu
Mossie et al. [6]	Real 35-bus feeder, Bahir Dar, Ethiopia	0.8083 pu (VSI-based)

The 0.9178 pu minimum voltage obtained here is closely consistent with the 0.9081–0.9131 pu range reported by Dash, Mishra, and Abdelaziz [3] for real and standard Indian-context feeders of comparable size, supporting the physical plausibility of the simplified positive-sequence model used in this study despite its necessary approximations.

5. Economic Consideration

This study does not perform a quantified economic analysis, but the results carry a direct economic implication consistent with the framework used by Dash, Mishra, and Abdelaziz [3]: a D-STATCOM's higher capital and converter maintenance cost per installed MVAr, relative to a passive capacitor bank, must be weighed against the light-load overvoltage and loss penalty the fixed capacitor was shown to incur in Sections 3.1–3.2. For a feeder whose load varies widely over the day (as most distribution feeders do), the fixed capacitor's loss penalty at light load is a recurring operating cost, whereas the D-STATCOM's higher upfront cost is a one-time expense; a full lifecycle cost-benefit analysis — following the annualized-cost methodology of [3] — is identified as future work.

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6. Numerical Cross-Validation of the Solver Implementation

To check the backward/forward sweep (BFS) solver used for all results above against a coding error, an independent Newton-Raphson power flow was implemented from the bus admittance matrix (Y-bus) of the same balanced positive-sequence network — identical topology, branch impedances, and loads, but a completely different numerical method (full Y-bus formulation with a numerically-differentiated Jacobian, rather than the ladder-iteration BFS approach). Both solvers were run independently on nine representative cases (loading levels of 25%, 60%, and 100%, each under all three compensation strategies) and their bus voltage magnitudes compared at all 13 buses.

Table: 6

Load (%)	Mode	BFS V_{675} (pu)	Newton-Raphson V_{675} (pu)	Match
25	None	0.9811	0.9811	✓
25	Fixed capacitor	1.0225	1.0225	✓
25	D-STATCOM	1.0000	1.0000	✓
60	None	0.9529	0.9529	✓
60	Fixed capacitor	0.9963	0.9963	✓
60	D-STATCOM	0.9963	0.9963	✓
100	None	0.9178	0.9178	✓
100	Fixed capacitor	0.9640	0.9640	✓
100	D-STATCOM	0.9640	0.9640	✓

Across all nine cases and all 13 buses (117 individual voltage comparisons), the maximum discrepancy between the two independently implemented solvers was 4.97×10^{-5} pu — consistent with the convergence tolerances used (10^{-9} pu for the BFS sweep, 10^{-7} pu for the D-STATCOM outer control loop) rather than any systematic disagreement. This is offered strictly as numerical cross-validation of the solver implementation — confirming the BFS code correctly solves the balanced positive-sequence network as it was defined in Section 2.1 — and should not be read as validation of the balanced positive-sequence simplification itself against the officially unbalanced IEEE 13-node feeder. That validation would require solving

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the full unbalanced model in dedicated distribution analysis software (e.g., OpenDSS, ETAP, or DIgSILENT PowerFactory), which was not available in the environment used for this study and is identified as priority future work in Section 4.

7. Limitations

- The IEEE 13-Node feeder is officially specified as unbalanced three-phase with a voltage regulator and an in-line transformer; this study uses a balanced positive-sequence equivalent, and the regulator and original capacitor banks are deliberately excluded to isolate the compensation-strategy comparison (see Section 2.1). The Newton-Raphson cross-check in Section 3.6 confirms the solver correctly solves this simplified network, but does not validate the simplification itself against the officially unbalanced feeder; that requires a full unbalanced solution in software such as OpenDSS, ETAP, or DIgSILENT PowerFactory, which was not available in this study's environment and remains the single most important item of future work.
- Line reactance is computed from official conductor GMR data using a representative, rather than the officially surveyed, phase spacing.
- The D-STATCOM is modeled as an idealized controllable reactive source with a simple droop law; converter losses, switching harmonics, and control-bandwidth limits of a physical device are not represented.
- Loads are modeled as constant-power (PQ); voltage-dependent load behavior is not considered.
- The siting comparison in Section 3.3 tests the feeder's eight load-carrying buses; the five zero-load junction/end buses (650, 633, 680, 692's switch node itself, etc.) were not separately tested as compensation sites since they carry no local demand of their own.

CONCLUSION

This study compared a fixed capacitor and a droop-controlled D-STATCOM of identical 1.5 MVAr rating on a positive-sequence equivalent of the IEEE 13-Node Test Feeder across ten loading levels and all eight of the feeder's load-carrying buses. The two devices perform identically once feeder loading exceeds their shared rating, but below that point the D-STATCOM's dynamic modulation avoids both the overvoltage (up to 1.0333 pu) and the counter-intuitive loss increase (over 15× at 10% load, concentrated in the trunk branches nearest the substation) that the fixed capacitor produces at light loading, while holding the

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compensated bus at exactly its 1.00 pu setpoint. A full siting sweep found that both the loss-reduction benefit and the crossover load level are strongly site-dependent: Bus 671, the feeder's main junction, gives the best loss reduction (28.3%, crossover at 60% load), while Bus 634, isolated behind the feeder's step-down transformer, gives the least (1.7%, never saturating even at full load) — indicating that D-STATCOM siting, not only sizing, materially determines the device's value over static compensation. The uncompensated sag magnitude obtained (0.9178 pu) is consistent with previously published results from real Indian and Ethiopian distribution feeders, supporting the model's physical plausibility, and an independent Newton-Raphson implementation reproduced the backward/forward sweep results to within 5×10^{-5} pu, confirming the load-flow solver itself is implemented correctly — though this does not substitute for validating the balanced-equivalent simplification against the feeder's official unbalanced specification. Future work should extend this comparison to a full unbalanced three-phase model of the officially configured feeder (including its voltage regulator) solved in dedicated distribution analysis software such as OpenDSS, incorporate a physical D-STATCOM converter and control-loop model, carry out a quantified lifecycle economic comparison between the two compensation strategies, and extend the single-device siting sweep in Section 3.3 toward a time-varying, multi-unit D-STATCOM placement study using particle swarm optimization, following the author's own prior convergence-analysis framework [11].

CONFLICT OF INTEREST AND DATA AVAILABILITY

The author declares no conflict of interest. The Python implementation of the load-flow model and all simulation data underlying this study's tables and figures are available from the author upon reasonable request.

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