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Silvaco TCAD based Analysis of Cylindrical Gate -All-Around FET Having Indium Arsenide as channel and Aluminium Oxide as Gate Dielectrics

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Abstract

In this work, a cylindrical gate-all-around (CGAA) FET (field-effect transistor) structure with Indium Arsenide (InAs) nanowire is used as channel instead of silicon nanowire, and aluminium oxide is used as the gate dielectrics instead of silicon dioxide. The performance of this setup was demonstrated using ATLAS simulator of Silvaco TCAD software. Indium Arsenide is chosen due to its high electron velocity, high saturation velocity and low contact resistance, whereas, aluminium oxide is chosen because of its higher permittivity. Simulation results indicate that the proposed combination is superior to the CGAA structures having channel-gate dielectrics that use combinations of silicon-silicon dioxide and Indium Arsenide-silicon dioxide. The effects of variation of nanowire radius, channel length and oxide thickness on the output and transfer characteristics curves, and also on the performance parameters such as maximum drain current, maximum transconductance, on resistance and inverse subthreshold slope are investigated to show the superiority of the proposed structure

***Keywords**: Cylindrical Gate All around MOSFET; Indium Arsenide nanowire; Aluminium Oxide; high-k dielectrics*

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INTRODUCTION

Short channel effects (SCE) become one of the major challenges in scaling down of MOSFET feature size in order to fulfil the requirements suggested by the International Technology Roadmap for Semiconductor (ITRS) for improved performance. Therefore, non-classical FET structures such as double-gate, triple-gate, FinFET, pi-gate, sigma-gate and gate all around FET structures are proposed in the literature, mainly to reduce SCE and hence, to extend the scalability of FET devices.

However, gate all around (GAA) structure based on MOSFET devices becomes the best alternative among these structures and hence, draws increasingly more attention of the researchers for their immunity of SCE and ultra-scalability [1]–[4], and also for their superb electrostatic control of the gate over the channel region owing to the reduced electron scattering [5]. Although GAA devices can be based of rectangular and cylindrical nanowires, the cylindrical one is a better option. Indeed, rectangular GAA FETs suffer from the lower current drive due to the fringing effects (also known as corner effects), but cylindrical devices have reduced corner effects.

In order to get better device performance as well to reduce the fabrication cost, different high-K gate oxides and high mobility channel materials are suggested in the literature. For this, we have paid paid attention to III-V semiconductors such as InAs, SnAs, InGaAs etc. as channel materials to get higher current drive for their extremely high electron mobility and low effective mass [6]. Of these, InAs is the most suitable as a channel material owing to its higher electron mobility (up to 30000 cm2/V-s), lower electron effective mass (0.023 m0), higher saturation velocity (2×107 cm/s) and low contact resistance [7,8].

On the other hand, high-k dielectric materials are strongly recommended to obtain higher gate capacitance as well as lower gate leakage current. Recently, some high-k dielectric constant materials such as Al2O3, HfO2 etc. are paying considerable interest as gate oxide. Do et al. [9] showed that when Al2O3 is selected as gate oxide with III-V based channel semiconductor layer during appropriate annealing process [10] of fabrication steps, no surface defects is observed and hence, a high quality dielectric film is resulted.

In the literature, a number of research works based on gate-all-around structures

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are proposed. Yi et al. [3] analyzed a GAA structure with Si-nanowire on bulk Si-substrates. Sofia et al. [1] and proposed a GAA structure with vertical InAs nanowire on Si substrates. The first CGAA structure based on InAs-nanowire as channel material and HfO2 as gate oxide is proposed by Jahurul et al. [8].

Although Al2O3 has lower permittivity than HfO2, gate oxide Al2O3 is still a better option as mentioned earlier. Therefore, in this work, a novel CGGA FET structure based on InAs-nanowire as channel material and Al2O3 as gate oxide is proposed. The proposed device structure is implemented using the ATLAS simulator of Silvaco TCAD software. The performance of this proposed structure, i.e. output and transfer characteristics and the various performance parameters (figures of merit) are obtained and also, the effects of channel length, channel radius, channel doping level and the oxide thickness are investigated. The results are compared with other channel/gate oxide combinations i.e. Si/SiO2 and InAs/SiO2 to assess the superiority of the proposed structure.

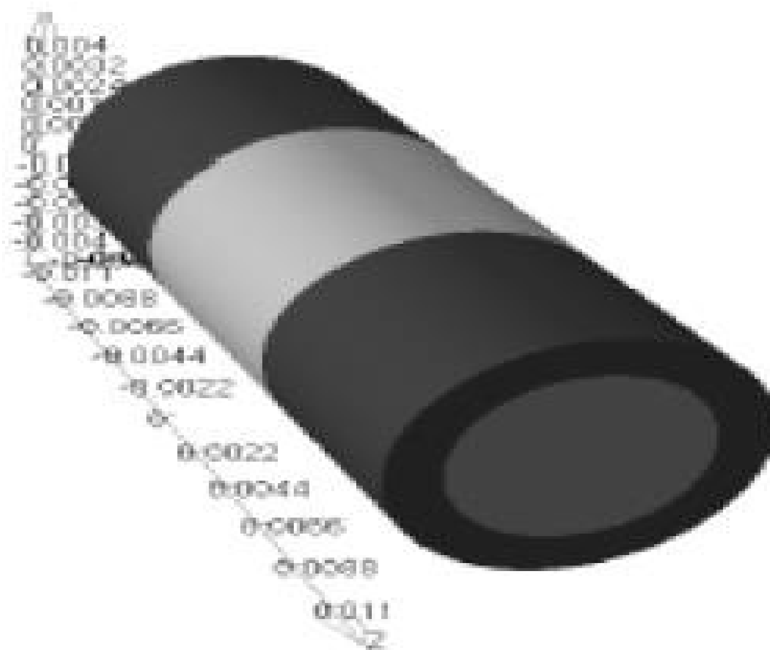

Fig. 1: 3D view of the proposed cylindrical gate-all-around MOSFET generated by ATLAS.

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A. Device Structure

The device structure proposed in this work has been simulated using ATLAS simulator of Silvaco TCAD. The generated 3-D view of this structure using ATLAS is shown in Fig. (1), where InAs-nanowire is shown as channel and Al2O3 as the gate oxide. Because of the cylindrical symmetry of the CGAA structure, quasi-3D model structure is used to simulate the structure in ATLAS. In the 'mesh' statement, this cylindrical symmetry is specified for which ATLAS simulates the structure so that its x-direction is in the radial direction of the cylinder, its z-axis is at the center of the cylinder, and its y-axis is in the downward direction with origin at the top of the structure. The 2D radial cross-section view is shown in Fig. (2). the device is implemented as doped source/drain type MOSFET. The channel length is varied in the range of 100-200 nm, whereas, the channel radius is varied between 10-20 nm. The gate oxide thickness is 4-12 nm. The channel doping level is varied from 1×1017 to 5×1018 cm-3.

B. Device Simulation

All the simulations are carried out using ATLAS of Silvaco TCAD. Fermi-Dirac statistics is used instead of Boltzmann statistics. Since the channel length and radius are of the order of 100 nm, field-dependent mobility needs to be considered.

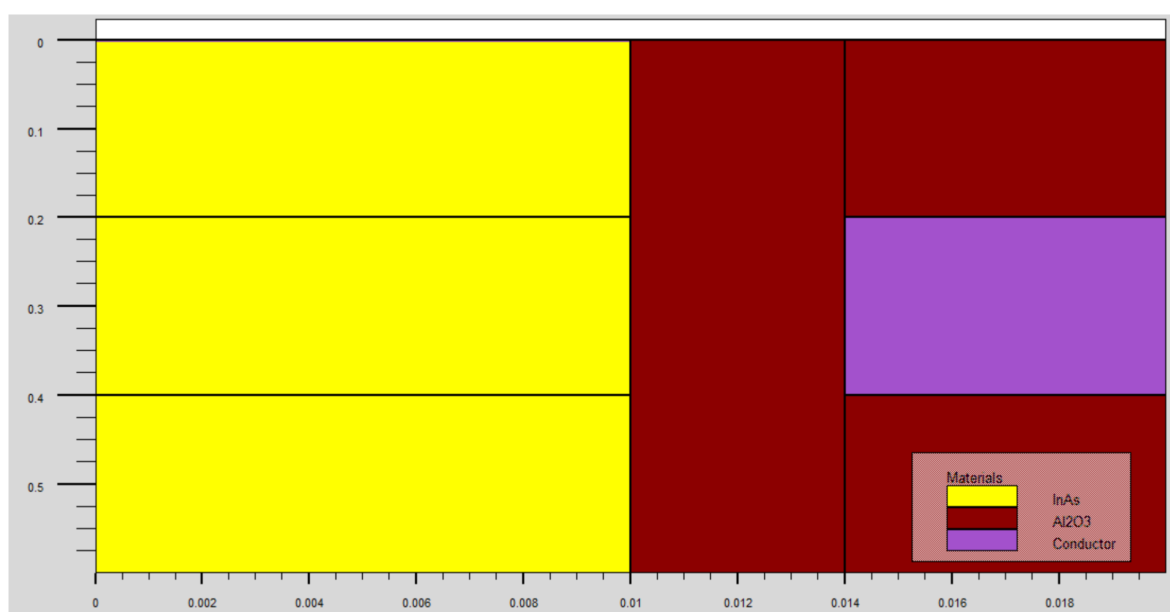

Fig. 2: 2D radial cross section view of the proposed cylindrical gate-all-around MOSFET generated by ATLAS.

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Therefore, field-dependent mobility models are included in the analysis. The band profile InAs is chosen as 1D as suggested in [11]. For recombination models, Shockley–Read–Hall (SRH) recombination mechanism is considered. For the sake of simplicity, simple drift-diffusion model is used.

For numerical iterations, both Newton and Gummel methods are applied. However, in order to speed up the iteration process, automated Newton-Richardson procedure is implemented.

RESULTS AND DISCUSSION

This section presents and analyses the simulation results carried out by the ATLAS simulator of Silvaco TCAD software for the output characteristics (ID vs. VD) and the transfer characteristics (ID vs. VG) and for the various figures of merit and also, discusses the effects of various parameters on these curves and figures of merit of the proposed CGAA structure. In order to assess the superiority of the proposed structure, this section also presents a comparative analysis between the proposed structure with two other GAA structures having the channel-gate oxide combinations of Si-SiO2 and InAs-SiO2.

Figs (3), (5) and (7) show the output characteristics (ID vs. VD) and figs. (4), (6) and (8) show the transfer characteristics (ID vs. VG) for three GAA structures having different channel-gate oxide combinations. From all these figures, it is clearly evident that the proposed CGAA structure having InAs as channel material and Al2O3 as gate dielectrics outperforms the other CGAA structures. This is because of the fact that the electron mobility (µn) in the InAs channel is more than 60 times higher than that in the Si-channel (µn,InAs = 80000 compared to µn,si = 1300) and the relative permittivity (εr) of Al2O3 is roughly three times higher than that of SiO2 (εr,Al2O3 = 9.00 compared to εr,SiO2 = 3.90). Indeed, the drain current of the GAA FET is directly proportional to both the electron mobility in the channel and the permittivity of the gate dielectrics. Therefore, the drain current is higher for GAA structure having InAs-SiO2 channel-gate oxide combination and becomes the largest for InAs- Al2O3 channel-gate dielectrics combination.

An important observation has been made from the transfer characteristics curves [Figs. (4), (6) and (8) that the threshold voltage (which is the minimum gate voltage required to turn on the FET) is the

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highest for GAA structures having the Si-channel and SiO2-gate dielectrics combination and is lowered down for the GAA structures with InAs as channel material. It is noteworthy that the change of the gate dielectrics from SiO2 to Al2O3 does not change the threshold voltage at all.

The effects of the variation of the channel radius on the output and the transfer characteristics have been observed in Figs. (3) and (4). In both of these figures, it is seen that higher drain current can be obtained as channel radius increases. This is expected as the higher channel radius creates the wider cross-section for the current flow, thereby causing an increase in the drain current.

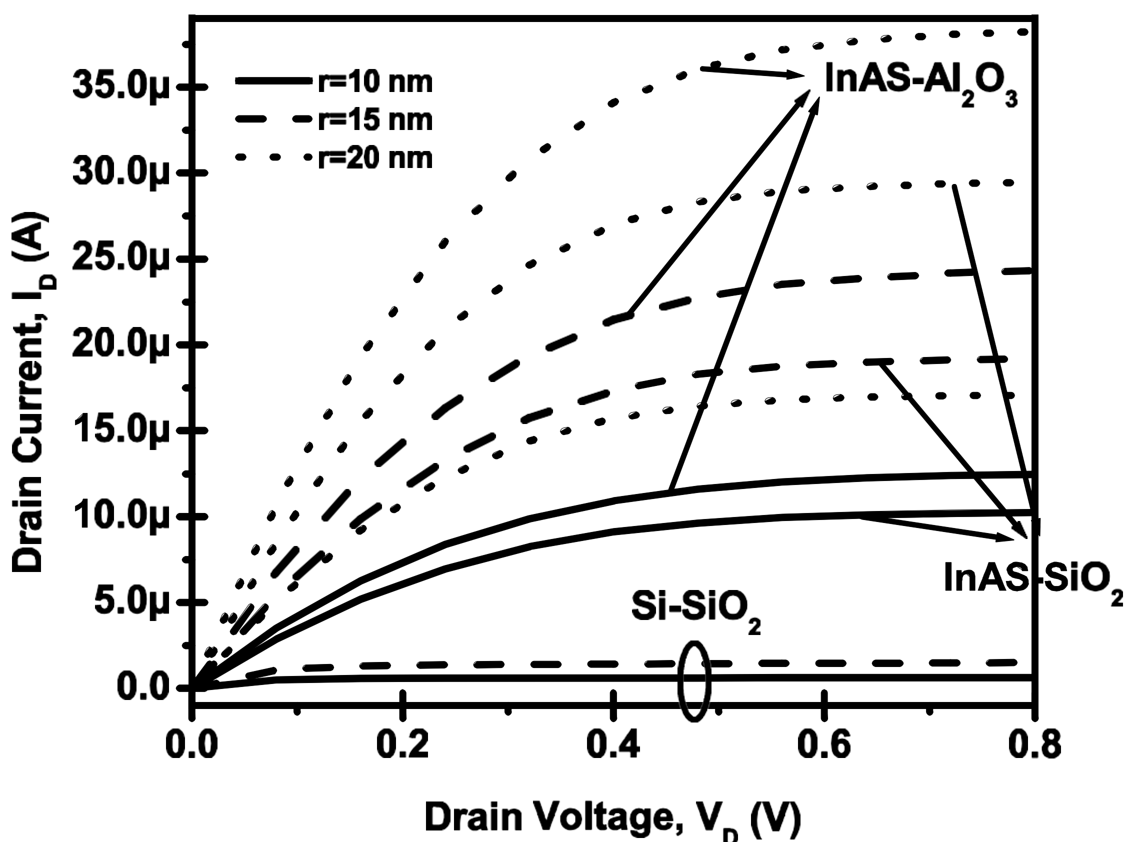

Fig. 3: Effect of variation of channel radius on the output characteristics at VG = 0.5 V. For all three structures, channel length is 200 nm, oxide thickness is 4 nm and channel doping level is 1×1017 cm-3.

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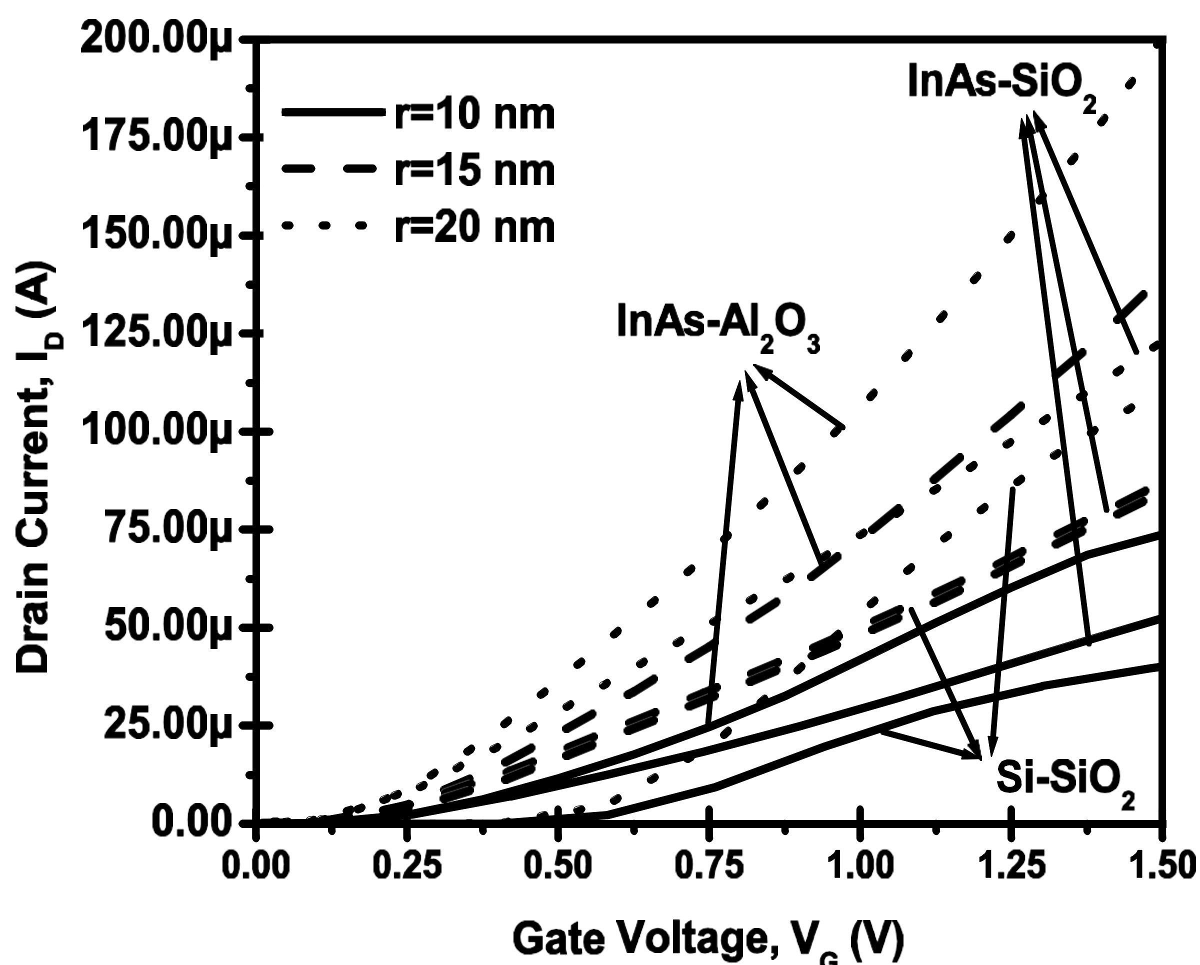

Fig. 4: Effect of variation of channel radius on the transfer characteristics at VD = 0.5 V. For all three structures, channel length is 200 nm, oxide thickness is 4 nm and channel doping level is 1×1017 cm-3.

Figs (5) and (6) display the effects of channel length variation on the ID vs. VD and ID vs. VG characteristics curves. Since larger channel length provides a longer path for the carriers to reach the drain end and causes the same amount of the drain, the current for longer channels is lowered. This fact of lowering drain current as channel length increases is evident from both the output and the transfer characteristic curves for all three GAA structures

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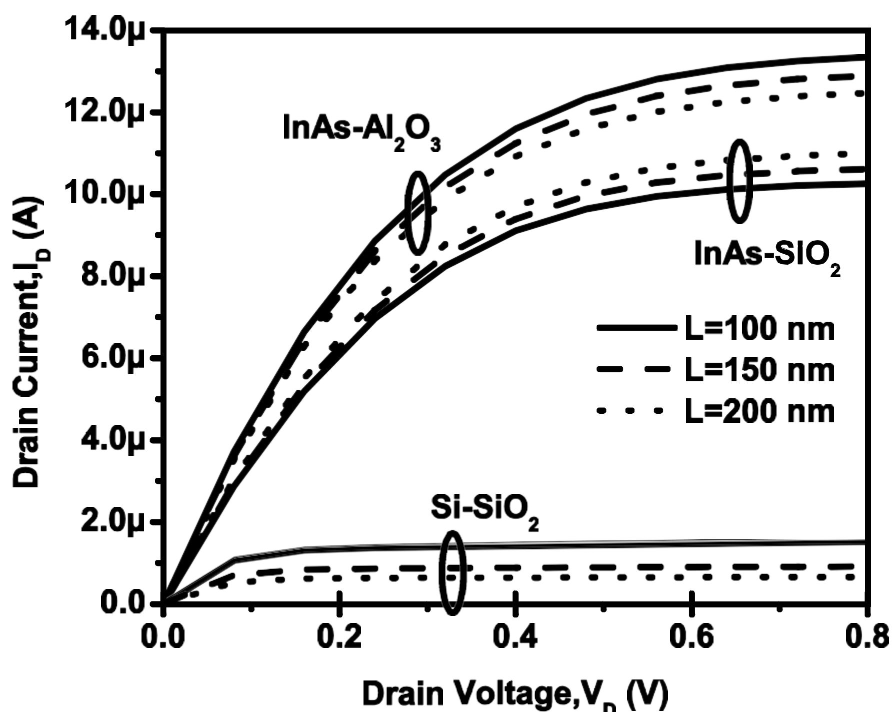

Fig. 5: Effect of variation of channel length on the output characteristics at VG = 0.5 V. For all three structures, channel radius is 10 nm, oxide thickness is 4 nm and channel doping level is 1×1017 cm-3.

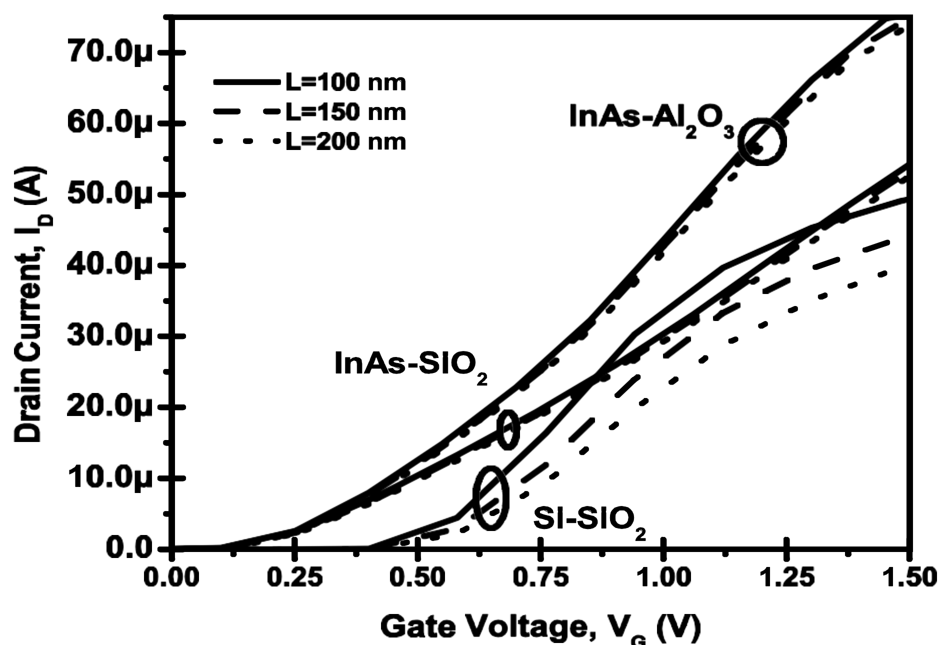

Fig. 6: Effect of variation of channel length on the transfer characteristics at VD = 0.5 V. For all three structures, channel radius is 10nm, oxide thickness is 4 nm and channel doping level is 1×1017 cm-3.

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The thickness of the gate oxide (TOX) has a strong effect on both of the output and the transfer characteristics, since TOX is inversely proportional to the oxide capacitance, which is directly proportional to the drain current. Therefore, decrease in the TOX increases the gate capacitance, thereby causing an increase in the drain current. This phenomena can also be observed in the Figs. (7) and (8).

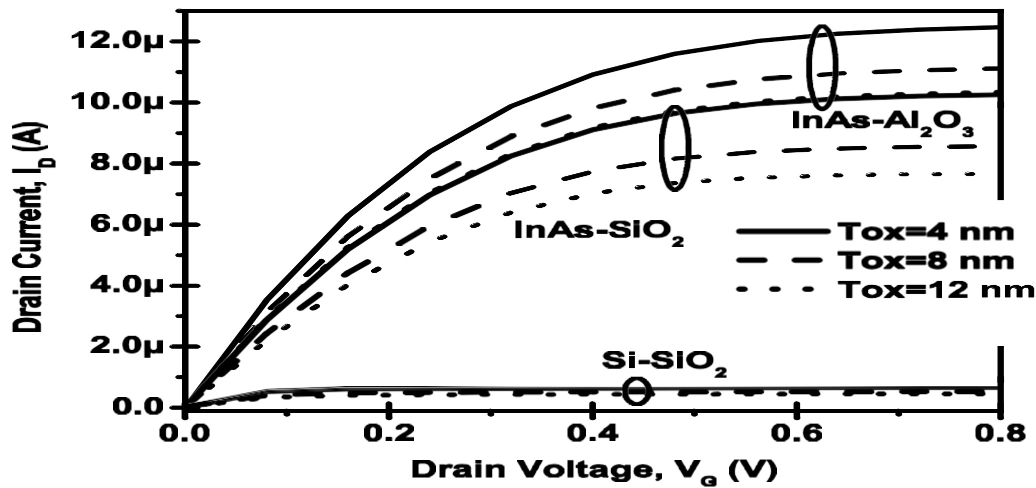

Fig. 7: Effect of variation of oxide thickness on the output characteristics at VG = 0.5 V. For all three structures, channel radius is 10 nm, channel length is 200 nm and channel doping level is 1×1017 cm-3.

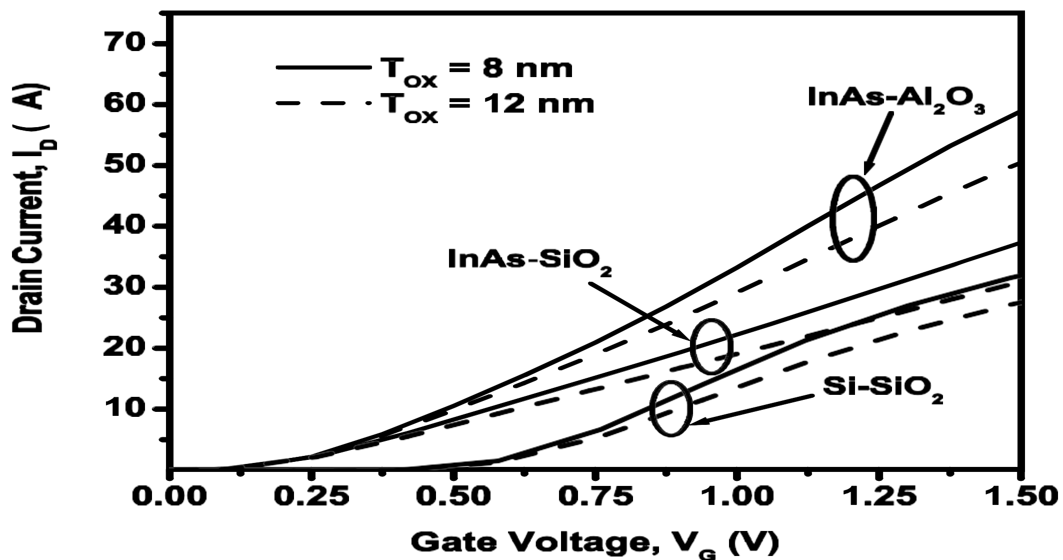

Fig. 8: Effect of variation of oxide thickness on the transfer characteristics at VD = 0.5 V. For all three structures, channel radius is 10 nm, channel length is 200 nm and channel doping level is 1×1017 cm-3.

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Table 1. Comparative analysis of figures of merit for the three CGAA structures mentioned in this work. For all three structures, channel radius is 10 nm, channel length is 200 nm, oxide thickness is 4 NMAND channel doping level is 1×1017 cm-3.

Figures of Merit	**CGAA Structures**		
	Si-SiO₂	***InAs-SiO₂***	***InAs-Al₂O₃***
$g_{m,max}$ (mS/μm)	0.8562	0.75	1.2
I_{max} (mA/μm)	0.01015	0.164	0.197
R_{ON} (Ω-μm)	9927	1929	1433
I_{SS} (mV/dec)	60.5	63.3	62.2

However, inconsistency in the ISS values can be attributed to the presence of excessive trap charges at the oxide-semiconductor interface for InAs-channel based FETs compared to the Si-channel based FETs. However, InAs-Al2O3 channel-dielectric combination based CGAA structure is the best among all the structures mentioned in this work. It has ISS, although degraded, that is close to the theoretical lowest limit of 60 mV/Dec.

CONCLUSION

In this work, a cylindrical gate-all-around FET structure having InAs-nanowire as channel and Al2O3 as gate dielectrics have been simulated, analyzed and investigated using Atlas of Silvaco TCAD software. The proposed structure shows superior performance than the CGAA structures when either the channel is replaced by InAs or the gate dielectrics are replaced by SiO2. Based on ATLAS simulations, the new structure shows the lower threshold voltage, the higher drain current, comparatively lower inverse sub-threshold slope, lower on-resistance and higher maximum transconductance. Effects of the variation of channel radius, channel length and the gate oxide thickness on the characteristic curves and on various figures of merit show consistency with the physical insight.

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