

Review on Performance Analysis of LNA for 2.4 GHz RF Receiver Front End using 180 nm CMOS Technology

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Abstract

This Paper presents the reviews of few previous works for low noise amplifier(LNA).This paper will explore recent architectures of LNA and Gm-boosting and current reuse techniques .These techniques are useful for better noise figure, increasing gain, and good impedance matching. As to improve the above parameters further an inductor connected at the gate of the cascode transistor and capacitive cross-coupling is reviewed. In this survey we try to use a technique to improve the gain, increase the linearity and Noise figure of LNA and study various design parameter improvement techniques using supply voltage of 1.8 V for 2.4 GHz RF receiver.

Keywords: *Low Noise Amplifier; RF CMOS; Linearity; Noise figure; Transceiver*

I. INTRODUCTION

CMOS RF integrated circuits (RFIC) for wireless communication in the 2.4 GHz frequency range have received much more interest owing to their potential low cost, low power and the prospect of system level integration. Low cost, low power can be achieved by integrating all the required blocks in the front-end of a

receiver as much as possible, thus minimizing the numbers of off-chips components. The heterodyne receiver architecture is the most widely used RF architecture for wireless applications because of sufficiently low noise figure. Figure1 shows a simple block diagram of a typical architecture of a heterodyne receiver. One of the most challenging

building blocks in the front-end receiver is the low noise amplifier (LNA) which precedes a high noise stage such as image rejection filter or mixer, etc.

The LNA determines the signal to noise ratio (SNR) of the whole receiver band. The basic function of the LNA is to provide signal amplification while adding as little noise and distortion as possible to improve the overall noise figure and linearity of the front-end. Receiver consists of various elements such as low noise amplifier, mixer, filter, local oscillator as shown in **fig 1**.

1.1 About Low Noise Amplifier

Low Noise Amplifier (LNA) is the first stage of radio receiver whose main function is to amplify the input signal to overcome the noise generated in the

following stage of the system, while adding as little noise as possible. It is the first gain stage after antenna in the receiver path, so the noise figure of LNA is the main factor in overall noise figure of receiver, since it directly adds to the total noise figure of whole system, and can approximated according to the Friis formula.

$$NF_{rec\ front} = \frac{(NF_{subsequent} - 1)}{G_{LNA}} + NF_{LNA}$$

Where $NF_{subsequent}$ is the total input referred noise factor of the components following the LNA, and G_{LNA} and NF_{LNA} are the gain and noise factor, respectively, of the LNA itself. The noise of all subsequent stages is reduced by the gain of LNA and the noise of the LNA is injected directly in to the received signal.

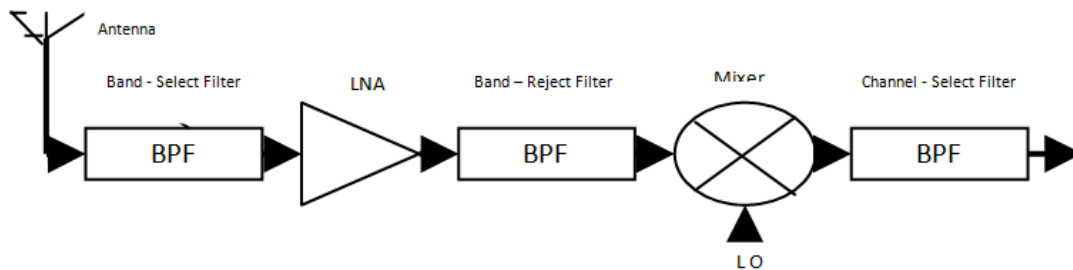


Fig 1 Block diagram of RF Receiver

Thus, the LNA needs both high gain and low noise. The inductively degenerated CS input consists of transconductors, M1–M2, and gate and source inductors, Lg and Ls respectively. The use of inductive source degeneration through Ls has the benefit of simultaneously achieving both input and noise matching. By employing this inductive source degeneration, a controllable real term in the input impedance can be generated as follows:

$$Z_{in} = \frac{V_{gs} + V_{gs}(S C_{gs} + g_m)(R_{ls} + S L_s)}{V_{gs} S C_{gs}}$$

$$= \frac{1}{S C_{gs}} + \frac{g_m R_{ls}}{S C_{gs}} + S L_s + R_{ls} + \frac{g_m L_s}{C_{gs}}$$

Hence, the input impedance is that of a series RLC network, with real part controllable by inductor value Ls. By choosing Ls properly, this real term can be made equal to 50-Ω. In most cases the input impedance Zin, is capacitive at the desired frequency of operation, and an additional inductor Lg, is added in series to provide resonance at the center frequency. Thus, the maximum signal is collected and gain could be optimized. To obtain power match at resonance the real part of Zin, must equal the source resistance Rs.

$$R_s = R_{ls} + \frac{g_m}{C_{gs}} L_s = \frac{W_0 L_s}{Q_{ls}} + \frac{g_m}{C_{gs}} L_s$$

For the noise figure (NF) calculation, the size of the input transistor is chosen such that it minimizes the noise as shown in the following expression:

$$F_{min} \approx 1 + \sqrt{\frac{4}{5} \frac{\omega}{\omega_T}} \sqrt{Y_8(1 - c^2)}$$

Where $\omega_T = g_m / C_{gs}$ the unity gain frequency with gm is the transistor transconductance and Cgs is the gate source capacitor. $c = 3/2$ is the channel thermal noise, c is the complex correlation term equal to j0.395, $d = 4/3$ is the coefficient of gate noise. It can be observed that Fmin is effective for $\omega < \omega_T$ and the NF increases with increasing the frequency. Fortunately, thanks to the long term trend of scaling CMOS processes to smaller geometries, the ω_T rises up and allows us to operate at higher frequency while maintaining minimum noise figure. Finally, having the Fmin at the frequency of interest, the optimal transistor size can be calculated in the following:

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_s}$$

with $R_s = 50\text{-}\Omega$ and L is the gate length. It must be noted here that in the above calculation the noise parameters, and c are considered as independent of the bias voltage.

2. LITERATURE REVIEW

The earlier techniques and concepts given by researchers are very helpful for analyzing the present high technology communication era. There is a growing demand of RFIC design to make device size small, portable and large frequency band applications. This paper presents brief review of the research done by various researchers in the area of designing of LNA by cascade stages, simple current reuse, source degeneration topology, resistive feedback, Gm-boosted topology, single stage, multistage designs which are the best design techniques. It is very essential to keep high gain with linearity and a low noise figure. The following literature review discusses all the above techniques.

LNA Architecture with comparison

The common LNA architectures can be categorized as:

- Resistive termination,
- $1/g_m$ termination,
- Shunt-series feedback and
- Inductive source degeneration

Resistive termination technique suffers from poor noise performance due to the deleterious effect of real resistor at input port. The $1/g_m$ termination method is more

suitable for bipolar transistor than CMOS to achieve low noise figure performance. Method of shunt-series feedback can increase the power dissipation compared to others with similar noise performance [5].

The inductive source degeneration method employs inductor at source terminal to generate a real term for the input impedance. This method often works with cascade transistor and has been widely used for LNA design due to its good noise performance, reverse isolation and high feasible gain. In this thesis inductive source degenerated LNA method is adopted for receiver front end.

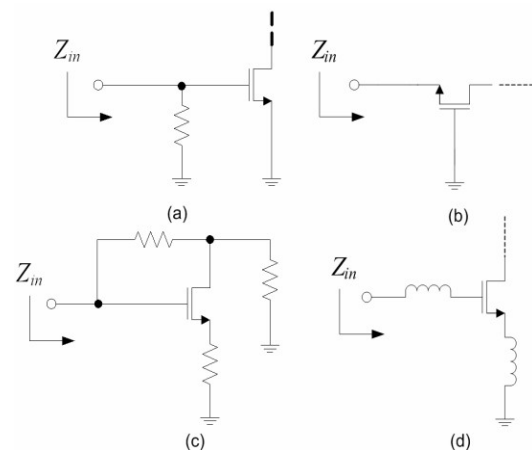


Figure 2: Common LNA Architectures
(a) Resistive termination (b) $1/g_m$ termination (c) Shunt-series feedback (d) Inductive source degeneration

Current Reuse Technique

In literature, several narrowband and broadband current-reuse architectures have been proposed and majority of them are based on a cascade of CS stages (CS-CS) sharing the bias current. A single inductor is used, to isolate the cascading stages adequately. Then for better isolation, in [3], LC T-network is used to provide third order isolation in the operating band along with improved noise performance. A narrowband gm-boosted CG LNA with current reuse technique is introduced which uses a CS amplifier as the cascaded stage (CG-CS) to boost the gain, in [5]. By using the transformer coils connected across the source and the gate terminals of the input device the gm-boosting gain is provided. Despite the transformer being a passive device consuming no electrical power, it is not suitable for adoption in UWB applications due to process nonlinearities and the presence of low parasitic resistance that can cause pronounced noise at the output of the amplifier. A gm-boosted CG UWB LNA is designed in [5], that utilizes an active pMOS CS device to provide the inverting gm-boosting gain. This design does not utilize the current-reuse technique and the bias currents through the CG amplifying stage and the CS gm

-boosting stage are not shared. It also utilizes another CS stage in cascade which is separately biased as well and because of that more power dissipation is there. The UWB LNA circuit, proposed in this paper, takes advantage of the current-reuse technique.

Thus the new approach proposed here, is to reduce the power dissipation associated with the gm-boosting, by implementing the “current-reused gm-boosting”, where the bias current is shared between the amplifier stage.

Gm-Boosting Technique

The gm-boosting stage made with a common source amplifier in [7]. In order to cancel the noise of CG transistor, instead of using feed-forward path, to cancel the noise of the input matching transistor we utilize gm-boosting stage. A way to reduce the noise factor of the common gate LNA is to increase the transconductance. The noise factor can be traded against input matching by increasing the transconductance i.e. increasing the current lowers the input impedance and the noise factor. A more clever way to do this is by inserting an inverting gain between the source and the gate node of the common gate LNA. Gm-boosting technique will be

employed which can effectively restrain the power, enhance the gain and reduce the noise simultaneously.

Different Types of LNA

As per the literature survey, the types of LNA are shown here. Each one has different feature.

Single Ended Topology

Single Ended LNA's are typically used in narrowband wireless applications. Inductively degenerated common source or common gate LNA topologies are the ones which are popularly used. Inductively degenerated common source (IDCS) amplifier has the best noise figure and provides both voltage as well as current gain thereby reducing the noise contribution to the succeeding stages. In Inductive source degeneration impedance matching is achieved without the use of a physical resistor which is advantageous as a resistor would add to the LNA's noise. The degeneration inductance has low impedance at low frequency, hence the topologies using inductive degeneration are more linear compared to those using resistive degeneration for the same biasing current. Some of the common source amplifiers utilize cascode connection. This type of topology reduces miller effect and improves LNA stability.

Common Gate LNA is also one of the popular topologies used in wireless communications. The common gate topology does not suffer from the miller effect. In CG stage the noise performance is independent of the operating frequency hence it is a suitable to use this configuration at higher frequencies

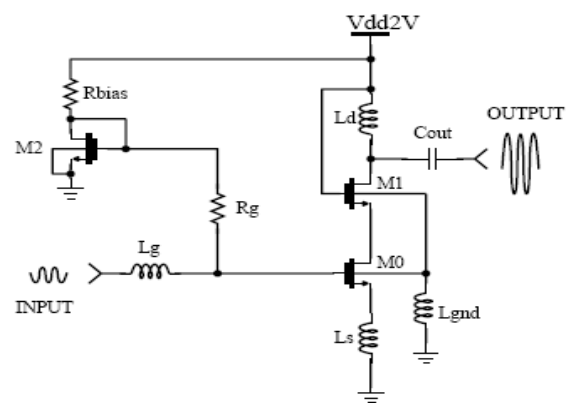


Fig 3: Schematic of a single ended LNA

Differential Mode Topology

Most of today's high performance wide-band amplifiers employ the differential topology. Although the single ended LNA topology consumes less power as well as less chip area sometimes at twice the cost the differential architecture is preferred. Noise figure is a critical factor for the low noise amplifier; the differential design has better noise performance due to the ability to reject common mode noise. Linearity wise the

differential LNA has a better performance because the circuit is symmetrical and natural ability to cancel out the even order distortions.

Differential topology is not only beneficial for sensitive signals but even for noisy signals. The total current drawn from the power supply is more or less constant and alternates between the two symmetrical branches of the differential amplifier which maintains a constant load to the power supply thereby reducing the noise generated in the power supply. Due to doubling of the devices in differential topology, the input noise voltage is $\sqrt{2}$ times in comparison to that in the single ended structure

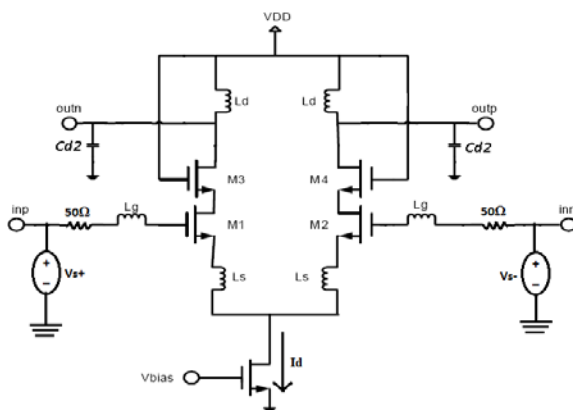


Figure 4: Differential LNA Topology

Muhammad Khurram and S. M. Rezaul Hasan, (2012) proposed a design that takes the advantage of the current- reuse

technique by “stacking” the active PMOS stage (that provides the inverting gm-boosting gain between the source and the gate terminals of the input CG stage) on top of the input CG stage (“piggyback gm-boosting”). The new proposed design reduced the power dissipation associated with the gm-boosting, by implementing the “current-reused gm-boosting”, where the bias current is shared between the gm-boosting CS stage and the amplifier CG stage. They represented a low-power CG UWB LNA architecture which implements a novel “current- reused-boosting” technique.

The topology also includes a front-end passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off. Proposed architecture represents a low-power CMOS transconductance “gm” boosted CG UWB LNA, operating in the 3–5 GHz range, employing current-reuse technique.[4]

Santosh B Patil, Rajendra D Kanphade, (2015) proposed a CMOS LNA that takes the advantage of Differential input differential output low noise amplifier working at 2.4GHz is designed using TSMC 180nm CMOS RF process.

Design methodology of LNA is analyzed in detail. Cascode topology with inductively degenerated common-source CMOS LNA is suggested with improved gain, linearity, stability and improved isolation. The optimum matching network is designed to minimize the noise figure (NF) and maximize the power gain. Layout is presented.

Pre layout and Post layout results are validated using Cadence Virtuoso IC 613. The proposed LNA exhibits a linear power gain of 14.55 dB, noise figure of 1.209 dB, input return loss (S11) of -14.15dB, Output return loss (S22) of -10.6dB and Isolation (S12) of -19.46dB and consume 3mA current at 1.8V supply voltage. Layout size is 0.261mm x 0.202mm.[5]

3. PROPOSED METHODOLOGY

The CG-LNA can achieve wideband input impedance matching, but suffers from poor noise performance. To alleviate this problem, a capacitive cross-coupling technique was proposed in for CG-LNA. It can boost the transistor transconductance with passive capacitors. If the gate-bulk and gate-drain capacitances are ignored, the effective transconductance and input

capacitance of the LNA are here derived as:

$$G_{m,eff} = \frac{2C_c}{C_{gs} + C_c} g_{m1}$$

$$C_{in} = \frac{4C_c}{C_{gs} + C_c} C_{gs} = \frac{2G_{m,eff}}{g_{m1}} C_{gs}$$

When $C_g \gg C_s$ the effective transconductance is doubled, and the input capacitance is increased by four times.

The inductively degenerated cascode CS-LNA can be considered as a CS-CG two stage LNA. The CS stage is designed to achieve the input impedance matching and also to obtain best noise performance. The input voltage signal is converted to current through the CS transistor. The cascode transistor works as a CG stage. It is designed mainly to reduce the Miller effect of the parasitic gate-drain overlap capacitance in the CS transistor. It also helps to increase the output impedance and to improve the input-output isolation.

An additional inductor L_{ack} combined with the capacitive cross-coupling technique is applied to the cascode transistors of the differential LNA to reduce the noise.

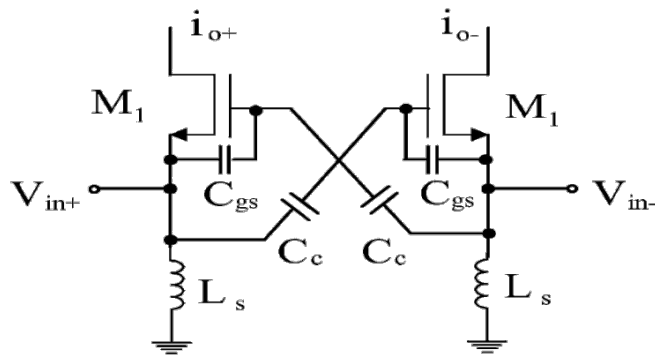


Figure 5: Proposed architecture of LNA

Table 1.1 Target specifications of the LNA

Categories	Specifications
Noise figure	$\leq 2\text{dB}$
S11	$\leq -10\text{ dB}$
S22	$\leq -10\text{ dB}$
IIP3	$\leq -10\text{ dBm}$
S21	$\geq 15\text{dB}$
S12	$\geq -20\text{dB}$
Input Impedance	50Ω
Output Impedance	50Ω

CONCLUSION

In this paper several techniques have been reviewed to impart high performance LNA design. In four techniques resistive termination, series shunt feedback, common gate connection and inductive degeneration that are used for matching,

the most efficient technique is inductive degeneration because during its analysis it provides resistive component in the absence of resistor. It reduces power dissipation and thermal noise. We try to present a new approach “Inductor connected at the gate and capacitive cross

coupling are combined” to reduce the noise further.

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