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Design and Implementation of Two-Dimensional Fast Lifting Wavelet Scheme for Image Compression

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Abstract

The lifting scheme is an implementation of Discrete Wavelet Transform. It presents primed computation of the wavelet coefficients. This paper presents Field Programmable Gate Array implementation of 2-D Discrete Wavelet Transform to compress the images for recovery and storage. The aim of this paper is to investigate novel and efficient Very Large Scale Integration designs for the lifting algorithm. The design is made in VHSIC Hardware Description Language using Xilinx ISE and the simulator used is ISE Simulator. The design can be used to reduce the complexity for lossy image compression. The Lifting Scheme has less memory requirement.

Keywords: *Discrete Wavelet Transform (DWT), Lifting Wavelet Transform (LWT), Field Programmable Gate Arrays (FPGA), Daubachies (9, 7) Filters, Very Large Scale Integration (VLSI), VHSIC Hardware Description Language (VHDL).*

I. INTRODUCTION

As a method, it was developed to acquire specific properties for a given wavelet transform. Two lifting algorithms are defined for its approach, one for lossless compression and another for lossy compression (1). Computational complexity of the lifting algorithm for lossless compression is relatively low. In this paper, we design rational lifting coefficients for filters to reduce the complexity for lossy compression.

The main aim of the paper is to examine novel and efficient VLSI designs to reduce the complexity for lossy compression in the lifting algorithm. The proposed architecture is well suitable for real-time applications which forms very low bit rate to high bit rate (6). Comparing with traditional Mallet Construction of WT, the lifting scheme is completely based on construction in spatial domain and it does not depend on the concept of translates and dilates.

Daubechies and Sweldens confirmed that any wavelet with FIR filters can be factorized into a predetermined number of lifting steps and all the conventional WT based on Mallet algorithm may locate their equivalent lifting scheme (2)(5). At first, some results are repeated to produce a complete understanding of the final implementation. Therefore, it is described how a discrete wavelet transform can be computed using the popular Mallet Algorithm. The Algorithm employs FIR filters and sub-samples of their output. Since the filters are orthogonal, they may be transformed based on a new wavelet design and computation approach, called Lifting Scheme. It reduces the computation level.

Lifting Scheme representation of the popular Daubechies-4 (D4) Wavelet filter will be derived. Several wavelet processor architectures are proposed in the literature and two of them will be revised and compared. These results will be used to initiate a new approach. The proposed architecture is based on the Lifting Scheme and having reduced computational demand. The design will emphasize on the different aspects of a VLSI implementation. The aim is to develop a processor being able to perform a lifting wavelet transform on input signal (9).

The input data has succeeding discrete time samples. It is possible a single chip realization of the processor with recent technologies. Therefore, the design process should consider the number of computation units, signal routing requirements, input/output data rate and storage space. The storage space might be independent of input data length.

2. LOSSY IMAGE COMPRESSION

Lossy image compression provides suitable image quality even dramatic reductions in image size. The wavelet transform has confirmed to be an essential tool in data compression for its ability to decorrelate data effectively and efficiently (3). For designing modified biorthogonal wavelets, the lifting scheme is very simple method and it has the numerous advantages (4):

- Saves storage by giving an in-place calculation of the wavelet transform

- Provides a normal way to introduce and think about wavelets.

Field Programmable Gate Array

FPGA abbreviates Field Programmable Gate Array, an integrated circuit especially designed to be configured by a designer or customer after its manufacturing and hence it is called as "field-programmable".

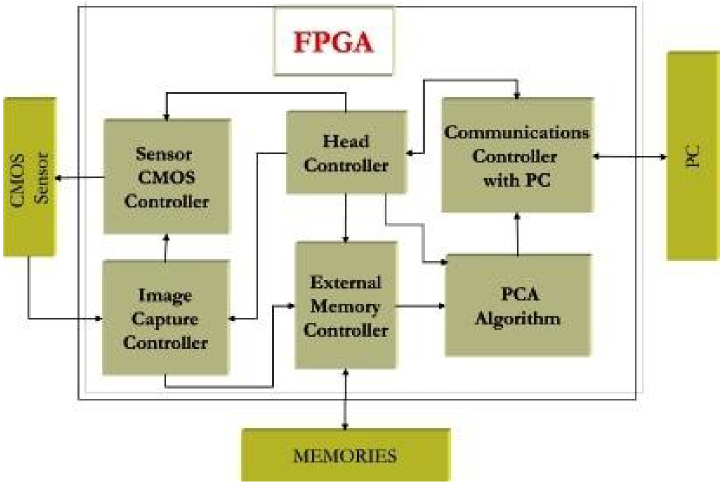

Fig. 1 Block Diagram of FPGA

Projected Architecture

FPGA is connected to the PCI bus trough a 32-bit wide local bus with a maximum frequency of 40MHz. The external SRAM located on the prototyping card is connected via a 36-bit wide bus and 21-bit address lines and several control signals. The pixels of an image can be transferred to the FPGA in a data stream with 4 pixels at one clock cycle, if we consider at most 8-bit grey scale or 24-bit color images. The maximal throughput is therefore given as 152 Mbytes per second and already bounded by the maximal throughput of the PCI bus of 132 M byte/s.

Generally, the projected architecture for the partitioned 2D-DWT consists of two one-dimensional DWT units (1D-DWT) for horizontal and vertical transformations, a control unit realized as a finite state machine and an internal memory block.

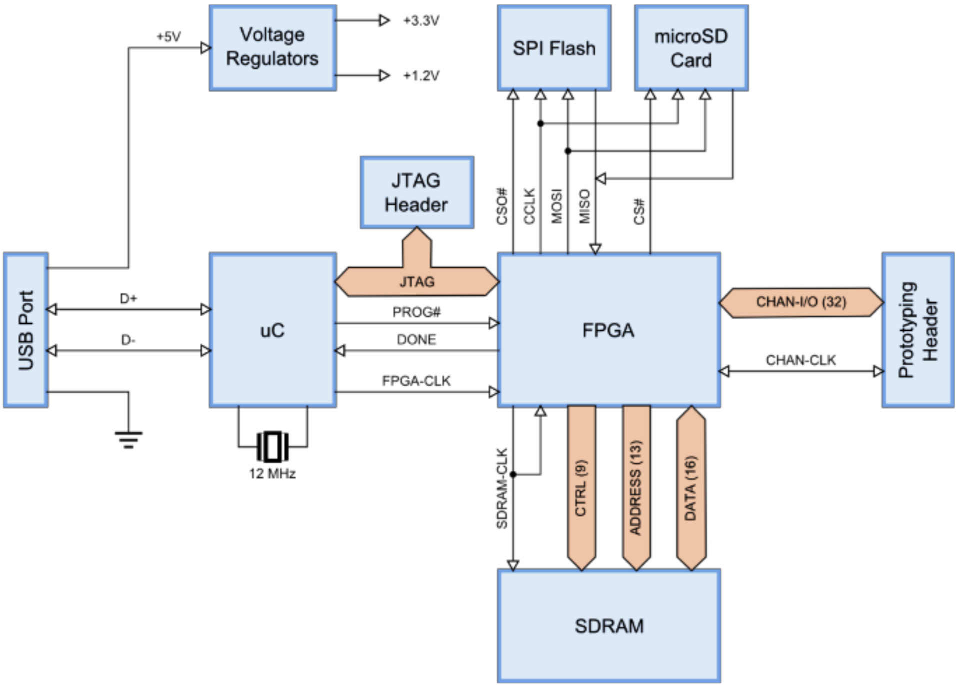

Fig. 2 Block Diagram of FPGA Prototyping card

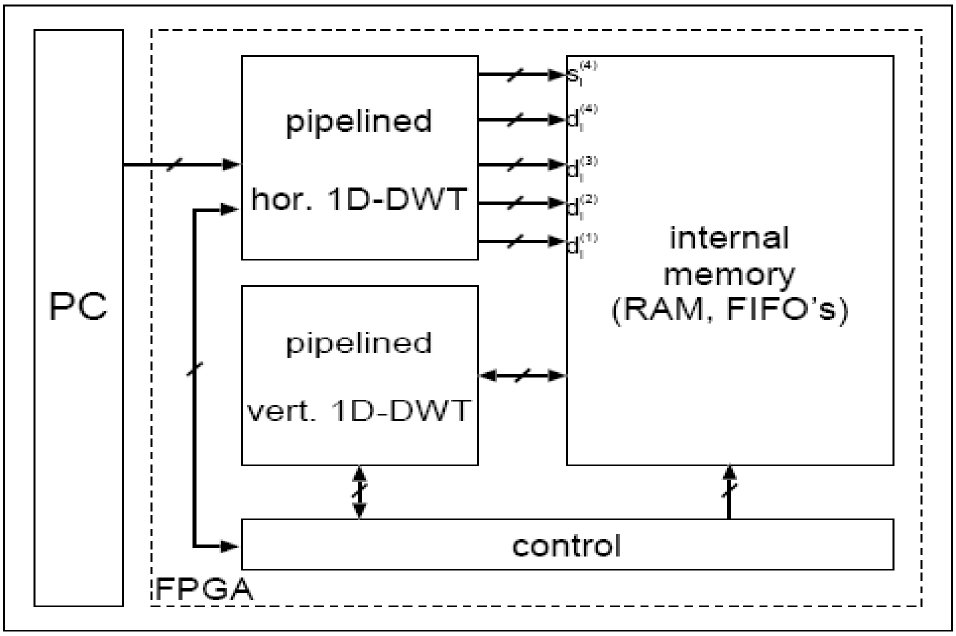

Fig. 3 Block Diagram of projected architecture

The coefficients computed in this way are stored in internal memory of different types.

The data throughput is generally dominated by the first stage, since the number of coefficients is down sampled to half after each level of transformation. So, the first two levels are performed by a module with higher throughput than the following two levels. At one clock cycle, the first and second stage outputs are two low frequency and two high frequency coefficients respectively.

After the first stage, two high frequency coefficients (the ones at even and odd positions) are combined together for continuous stream output. Similarly, the two low frequency coefficients are merged together. Further, they are combined into a four pixels wide bus as input of the second stage. This is done in the module named 2 to 4 by a simple delay element.

The second stage operates similar to the first stage at half of the speed only. The computed low frequency coefficients of two levels are merged together into a single data stream which is the input of third stage. The high frequency coefficients are merged in the same way and are shifted out. The transformation units of stage three and four take only one coefficient of the previous level as input and alternately the outputs are a low or a high frequency coefficient at one clock cycle. The horizontal 1D-DWT unit processes a pixel row of length 16 in only 32 input clock cycles including the boundary pixel.

3. LIFTING SCHEME

The lifting scheme is entirely based on the construction in spatial domain. The main scheme is found on the theory of bi-orthogonal wavelets and perfect reconstruction filter bank. Daubechies and Sweldens proved all the conventional WT based on Mallat algorithm which finds their equivalent lifting scheme.

Composing of lifting scheme Generally, lifting scheme is composed of three steps:

1. Split/Merge
2. Prediction
3. Update

Let $x_{(i)}$ denotes input signals.

1. Splitting

The input signals $x_{(i)}$ are separated into two sets of even and odd samples.

$$s_i^0 = x_{2i},\ d_i^0 = x_{2i+1}$$

2. Prediction

The odd samples are predicted by linear interpolation using coefficients *Pn* (*k*).

$d_i^n = d_i^{n-1} + \sum P_n(k)\, s_k^{n-1}$ where, $n=1,2,\ldots\ldots\ldots N$

3. Update

The even samples are updated with coefficient *Un* (*k*).

$s_i^n = s_i^{n-1} + \sum Un(k)\, d_k^n$ where, $n=1,2,\ldots\ldots N$

The prediction step and the update step may be performed in N sub-steps. The number of sub-steps N and the values of Pn (k) and Un (k) are depending upon the wavelet filters.

Normalization

Low pass and high pass outputs should be normalized to attain the exact results.

$s_i^N = K_0 s_i^n, \quad d_i^N = k_1 d_i^N$

Then the next transform step can be performed, but only using the low-frequency component just as WT. The lifting scheme of decomposition and reconstruction for 1-D signal is illustrated in the following figure.

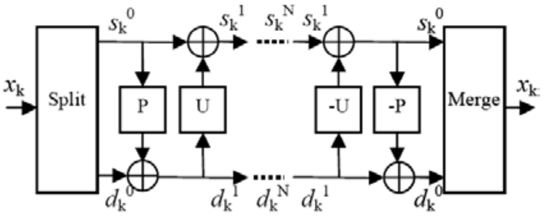

Fig. 4 Lifting scheme architecture

4. DAUBACHIES (9,7) FILTER CO-EFFICIENTS

Daubechies (9,7) serves as wavelet basis to construct the algorithm of LWT.

Start from the analysis filter:

$H_e(z) = h_4(z^2 + z^{-2}) + h_2(z + z^{-1}) + h_0$

$H_o(z) = h_3(z^2 + z^{-1}) + h_1(z + 1)$

Co-efficients are found as☐

$\alpha = h_4 / h_3, \beta = h3 / r_1, \gamma = r_1 / s_0, \boldsymbol{\delta} = s_0 / t_0, \delta = t_0$

where,

$r_0 = h_0 - 2h_1h_4/ h_3$

$r_1 = h_2 - h_4 - h_1h_4/ h_3$

$s_0 = h_1 - h_3 - r_0h_3/ r_1$

$t_0 = r_0 - 2r_1$

Table.1 Daubachies lifting co-efficients

Parameter	Value
α	-7/4
β	-1/23

γ	529/512
δ	128/299
δ	13/16

5. METHODOLOGY

The JPEG image will be read from the MATLAB file in the pixel value of 256 × 256.

By using the data converter software, the input image is converted into hex format. The Wavelet Transform is to be applied to this hex file. Thus, the image gets converted into different wavelet coefficients.

The transformed image is given to the data converter software once again which will produce the output image. It consists of large quantity of low frequency coefficients and low value of high frequency coefficients as compared to input image.

The VHDL code will be generated for the fast lifting wavelet transform scheme. The code is compiled and simulated using XILINX SPARTEN 3E.

Then, the codes will be synthesized by using synthesis tool which produces the fast lifting wavelet transform based architecture for VLSI implementation.

The design codes of fast lifting wavelet transform will be downloaded into FPGA for analyzing the design functionality.

Table.2 shows the computational cost of lifting algorithm versus standard algorithm with speed up.

Table.2 Computational cost of lifting algorithm versus standard algorithm with speed up

Wavelet	Standard Algorithm Cost (S)	Lifting Algorithm Cost (L)	Speed up
Haar	3	3	0%
D4	14	9	56%
D6	22	14	57%
(9-7)	23	14	64%

7. LIFTING SCHEME IMAGE IN MATLAB

Fig. 5 Input image – Lena (256x256)

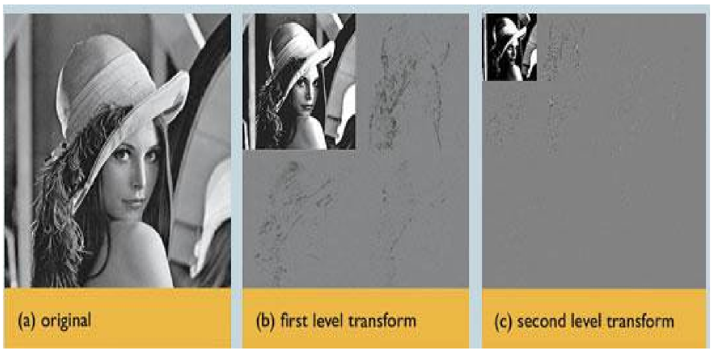

Fig. 6 Images with two levels of lifting

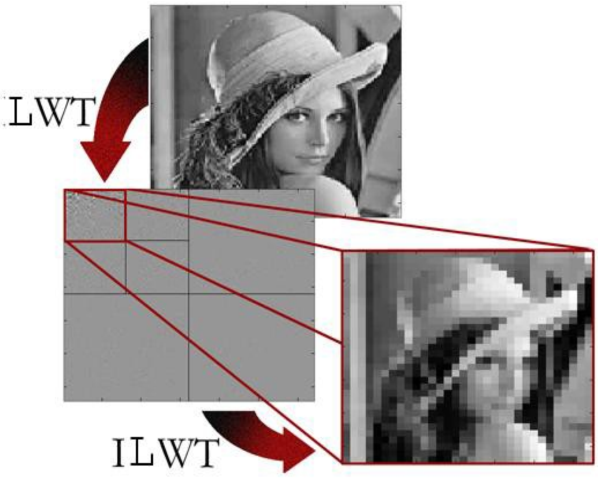

Fig. 7 Lifting wavelet transformation

CONCLUSION

This paper represents a VHDL architectures and implementation ideas for the lifting scheme. The architecture is developed for lossy compression, which is based on the lifting algorithm of wavelet Daubechies (9, 7) filters. The new whole integer processing of the wavelet transform scheme compression can be very useful in real-time application systems due to its high speed operation. The advantages of lifting scheme are less operation, in-place computation and less memory requirement.

The traditional advantages of lifting schemes are

Few developments of lifting which are currently under investigation are as follows:

1. Wavelets on general Surfaces:

The construction of spherical wavelets does not rely on the special properties of sphere. It uses only in fact that one can recursively cut the sphere into spherical triangles. Therefore, the construction can be generalized to more general surfaces or manifolds.

2. M-band Wavelets:

Several prediction and update operators can be used.

3. Wavelet Packets:

The lifting scheme can also be used in the construction of wavelet packets.

4. Wavelet Frames:

The lifting scheme can be used to construct over complete representations or frames. Prediction and updating would lead to wavelet frames.

REFERENCES

I. A. Grzeszezak, M. K. Mandal, S. Panchanathan, T. Yeap, IEEE transactions on VLSI systems, Vol. 4, No 4, pp 421-433,December 1996.

II. A.R. Calderbank, I. Daubechies, W. Sweldens, et.al, Applied and Computational Harmonic Analysis, Vol. 5, pp. 332–369, 1998.

III. Colm Mulcahy, Spelman Science & Math Journal, Vol 1, No 1, April 1997, pp. 22-31.

IV. Fan Wenbing, Gao Yingmin, “FPGA Design of Fast Lifting Wavelet Transform”, Proceeding of IEEE Congress of Image and Signal Processing, 2008. DOI: 10.1109/CISP.2008.239

V. IEEE Workshop on Signal Processing Systems, 2000. DOI: 10.1109/SIPS.2000.886705

VI. M.Y. Zhu, Y.L. Zhao, “An Efficient FPGA Design for Lifting Wavelet,” International Conference on Computational Electromagnetics and Its Applications Proceedings, pp. 508-511, 2004. .

VII. Prachi Mukherji and Vaishali Gapchup, "Survey of Wavelet Transform and Applications”. Proc. of IEEE IMAE-05, Pune, 2005, pp. 20-24.

VIII. Stephen M. Trimberger, Proceedings of the IEEE, Vol. 103, No. 3, March 2015.