High Efficiency Solar Energy Harvesting IC for Biomedical Implant Applications

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Abstract

In this paper, high efficiency single-chip solar energy harvesting IC using on-chip solar cell for biomedical implant applications is presented. By inserting an on-chip charge pump with parallel connected photodiodes, a 3.5× efficiency improvement can be achieved when compared with the conventional stacked photodiode approach to boost the harvested voltage. A photodiode-assisted dual startup circuit (PDSC) is also used to improve the area efficiency and increase the startup speed by 77%. High efficiency system is implemented on 0.18-µm CMOS technology and it occupies an active area about 1.54 mm2. Here on chip charge pump is used so we get maximum 67% efficiency with incident power 1.22 mW/cm2.

Keywords: *Single chip solar energy harvesting, on chip charge pump, Auxiliary charge pump, Photodiode-assisted dual startup circuit.*

1. INTRODUCTION

In e-healthcare system patient can monitor their own health status at home which include information about ECG, breathing glucose level and heart rate etc. Recently solar energy harwasting is used in biomedical implant applications includes intraocular pressure monitoring [1] and subdermal implant applications [2]. In many implantable device wires are used to provide power from and to the device, but due to that it has limited distance, provide power to the chip [3]. In many applications today batteries are used but batteries can be very hazardous if they leak within the body. Clearly, batteries have limited lifetimes and after some time will be fully discharged [4]. So we can use solar energy harwasting IC in biomedical applications but we need such IC which provides highest efficiency. By integrating CMOS circuitry and solar energy harwasting on same chip we can reduce the total area of chip. Photodiode provide voltage in between 0.3 to 0.4V. This is to small voltage we need a system which provide high output power. So for that various solutions are available like silicon on insulator with serial connected photodiode with separate substrate, due to separate substrate used it increased the cost of chip [5]. In [6] and [7] different approaches to serial connected photodiodes are used but due to single substrate limitation it is not used also it reduces the overall efficiency of chip. DC-DC converter is used to boost the voltage also inductor based boost converter is available but it requires large off chip components [8]. To solve this problem on chip charge with along with photodiode is used to increase the overall efficiency and to boost the voltage level [9]. Also low input solar energy harwasting is available which provides 0.15 V with dynamic biasing, it requires 6 off chip components which increase the complexity of circuit [10]. Complete die -stacked platform is used to boost the voltage level [11].

2. BLOCK DIAGRAM

In figure 1 shows the system architecture of solar energy harwasting IC used in subdermal implant application. It is responsible for harwasting the incoming solar energy, process the incoming solar energy and transmit wirelessly to the dedicated medical server for further analysis process. Solar energy harvest the incoming solar energy from on chip solar cell and provide power to the voltage reference, clock phase generator, auxiliary charge pump and main charge pump etc. In order to reduce the noise coupling on chip solar cell divided into three building blocks like DM, DP and DR.

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Voltage reference provides the reference voltage to the clock phase generator along with PDSC. PDSC is the photodiode-assisted dual startup circuit used to improve the startup failure problem from voltage reference block. Clock phase generator provides two different non overlapping clock pluses Φ1 and Φ2 from five stage ring oscillator. Level converter generates four high swing clock pluses Φx1/Φx2 and Φo1/Φo2 to main charge pump.

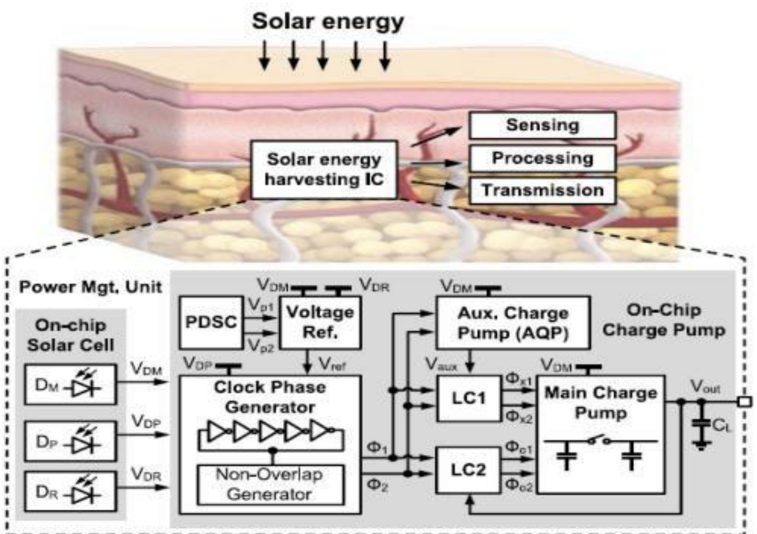

Figure 1 Solar energy harvesting IC used in subdermal implant application

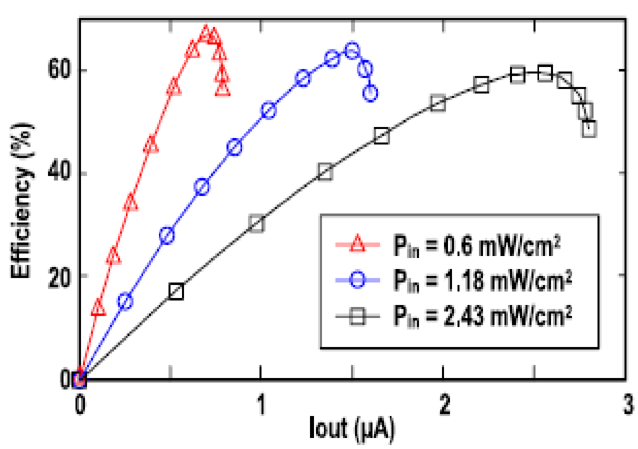

Figure 2 Measured efficiency under different incident power levels

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Table 1 Comparison with existing single-chip solar energy harvesting IC

	TED'12 [6]	TVLSI'11 [13]	TOBCS'17 [12]
Process (μm)	0.35	0.35	0.18
Light Source	White LED	Green Laser (532 nm)	Halogen Lamp
Incident Light Intensity	31 klx	34.2 μw	1.13 m/W mm^2
Area	0.69* ^{mm2} 1.38^ mm^2	338 μm^2	1.54 mm^2
V_{oc} (V)	0.52*	0.533	0.53
I_{sc} (μA)	17.5*	680	750
P_{out} (μW)	7.14*	225	322
Eff. (%)	9.5*‡	24	21.9*
Voltage Boosting	Stacked	-	On-Chip Charge Pump
$V_{out, boosted}$ (V)	0.97^†	-	1.08§
$Eff_{boosted}$ (%)	3.5^	-	12.1§

3. RESULTS AND DISCUSSION

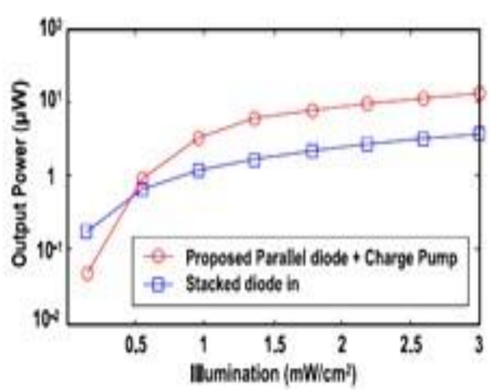

Figure 3 Power of the proposed photodiode with charge pump and the stacked photodiode

The single-chip solar energy harvesting system is designed and fabricated in a standard 0.18-μm CMOS process.. If incident power is less then we get maximum efficiency as incident power increases then efficiency of chip reduces [12]. Table 1 gives information about the performance comparison with existing single-chip solar energy harvesting IC. Conventionally, bootstrapping and ZVT switches are used for solar energy harvesting applications due to the low input voltage. This will increase the reversion loss due to the increased leakage and sacrificing the overall efficiency. The use of non-uniform gate drive voltages can also increase the conduction loss. To reduce these losses on chip charge pump along with ZVT switches are used. Figure 2 give information about haw input power affect on the overall chip efficiency. We can connect photodiode either parallel or stacked. If we connect photodiode in parallel along on chip charge pump we get maximum power, if we connect photodiode serially we get low output power shown in figure 3.

CONCLUSION

In this paper single-chip solar energy harvesting IC using on-chip photodiodes is explained. With the help of on chip charge pump and parallel connected photodiode we get 3.5 × improvements in energy harvesting efficiency. When we compared with stacked photodiode. Also due to use of PDSC circuit 77% efficiency improvement achieved. Use of on- chip charge pump along with zero threshold switches we can reduces the both inversion and conduction loss and achieve highest efficiency at the output.

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