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# *Wallace Tree Multiplier Design and Simulation with DNA Logic Gates*

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***Abstract***

*The DNA molecule is indubitably the most powerful medium known to code, store information as a means of data storage but till now, DNA molecule has found little use in computing applications. For initiating computing application with DNA molecule, it requires to design DNA transistors which can be utilized to design basic gates to implement Boolean logic. Interestingly, some recent researches have shown that it is very much possible to design a three terminal transistor like device architecture by controlling the flow of RNA polymerase along DNA with specific integrases as inputs. Such approach also initiated successful experimental design and realization of various basic Boolean logic Gates with DNA molecule. Present work theoretically adopted, modified and extended such DNA logic gate concept to execute design simulation of a 4*4 bit Wallace Tree Multiplier circuit. The timing diagram for input and product output has been successfully simulated which authenticate that such DNA logic gate concept can be extended to complex circuits also. The bit error rate and delay factor calculation have been done for the simulated circuit and approximate area analysis has been done. Present simulation model is designed with digital modeling approach in MATLAB Simulink with detail design methodology which will be a valuable step forward towards developing circuit simulator to simulate, analyze and fabricate bio-electronic circuits in near future.*


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***Keywords:*** *DNA, RNA, transcription, transistors, logic gates, wallace tree multiplier, simulation*

## INTRODUCTION

The world of electronics starts with a material called, „semiconductor", which can be shaped into a device to conduct or stop the flow of electrons or holes through a channel with precise control. Such silicon made three terminal device, transistor, has been the dominant electronics circuit component since the latter half of the 20th century [1].

In conventional electronic circuits transistors are assembled into higher order circuit components like logic gates to process, store and transfer signal or data. At the same time basic goal of the electronics industry is to process, store and transfer signal or data in large volume, with ultra high speed, consuming minimum power and cost [2]. Till now device designers have successfully executed this by scaling down the elementary transistor but such aggressive scaling action during decades has caused the transistor to reach its physical, technical and economic limits [3]. To overcome these limitations the scientists and technologists are looking for new materials, innovative structures and revolutionary ideas to realize reliable transistor like action [4]

On the quest to find new material and structure for transistors, recently several groups of scientists have engaged themselves to store, retrieve and process signals and data using bio-chemical reactions with newer biological materials [5–8]. With some breakthrough experimental research it has been successfully demonstrated that, the blueprint for life DNA, can also become the templates for making a new generation of transistors and logic gates [9–11].

Recently, Drew Endy et al. at Stanford University in California have experimentally realized logic gate like devices that controls the movement of an enzyme called RNA polymerase along a strand of DNA with bacteriophage serine integrases [12].

Such remarkable break through should be extended into the design and realization of higher order digital circuit which can be executed with experimental research along with theoretical modeling. But till now most of the research activities have been


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concentrated into intense experimental level [13–16]. The theoretical modeling and simulation of such logic gates and higher order circuits are highly essential to understand the circuit level performance of such new technology in comparison to the existing technology [17].

Not only that extending theoretical model into a simulator is also high on demand since such simulator will be immensely useful to design, analyze and realize the ultimate goal of future bio-electronic chip realization with DNA [17]. Keeping those goals in mind, under the present research, digital design of 4*4 bit Wallace Tree Multiplier (WTM) has been executed with DNA logic gates. The whole design has been logically realized with MATLAB Simulink. The input and product output for the DNA WTM has been simulated and verified with timing diagrams and truth table.

The bit error rate and delay factor calculation have been done for the simulated circuit and approximate area analysis has been done to understand its advantages over existing silicon technology. Such simulation work will not only justify the applicability of such DNA logic gate concept in complex circuit realization, it will also lead a step forward towards design and realization bio-chip and subsequent of Bio-electronic computer in near future.

## DIGITAL MODELING

The RNA polymerase is an enzyme that also known as DNA dependent RNA polymerase and it produces primary transcript RNA chains using DNA genes as templates, through a process called transcription [18]. The RNA synthesis or transcription process starts with the attachment of RNA polymerase to a specific site, “promoter”, on the template DNA strand and the synthesis process continues until a termination sequence (“terminator”) is reached [19].

The flow of RNA polymerase along DNA strands resembles like a current flow and can be named as transcriptional current. The gate like control can be realized with independent chemical input known as “integrase” which will regulate the flow of RNA polymerase along the DNA strands or transcriptional current to realize transistor or different Boolean logic operations (Figure 1) [12].


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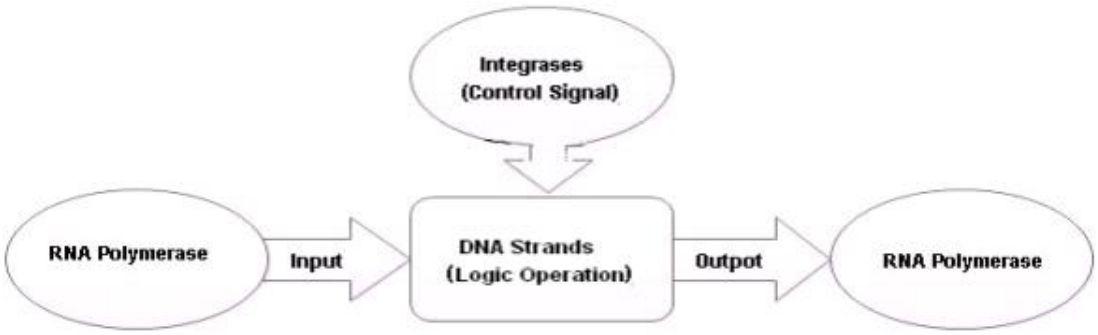



***Fig. 1: Schematic for Equivalent Logic Representation.***

As shown in the **"Figure 2",** the every logic element will use asymmetric Transcription Terminators (TT) as reversible check valves. A TT will be also coupled with a pair of DNA recombination sites named as Transcription Element (TE, LTE: Left Transcription Element and RTE: Right Transcription Element). Each TE may have opposing or favorable orientation and incase of opposing orientation it will disrupt RNA polymerase flow (as shown in Figure 2). The input integrase which is recombinases (genetic recombination enzymes), will catalyze unidirectional inversion of DNA coding within transcription terminator [12]. This will also modify opposing TE (represented with partially dark green-blue and partially dark blue-green solid triangles) and will allow RNA polymerase flow. Every TE will be recognized by independent integrase which will provide independent control over the orientation or presence of one or more terminators.

**Symbols:** LTE: Left Transcription Element, RTE: Right Transcription Element [20 –23].

## MULTIPLIER DESIGN

Multiplication is a commonly used operation in the digital computational arithmetic and the Multipliers based on Wallace reduction tree provide an areaefficient strategy for high speed multiplication [21]. Significant number researches have been carried out to optimize the performance of the Wallace multiplier [21, 22]. Considering those, under the present work, "Wallace tree multiplier", has been design with DNA logic gates which multiplies two four-bit binary numbers and produces output as the product of the two four bit inputs as shown in "Figure 3". A Wallace tree multiplier is composed with three basic digital units Full adders and Half adders [22].


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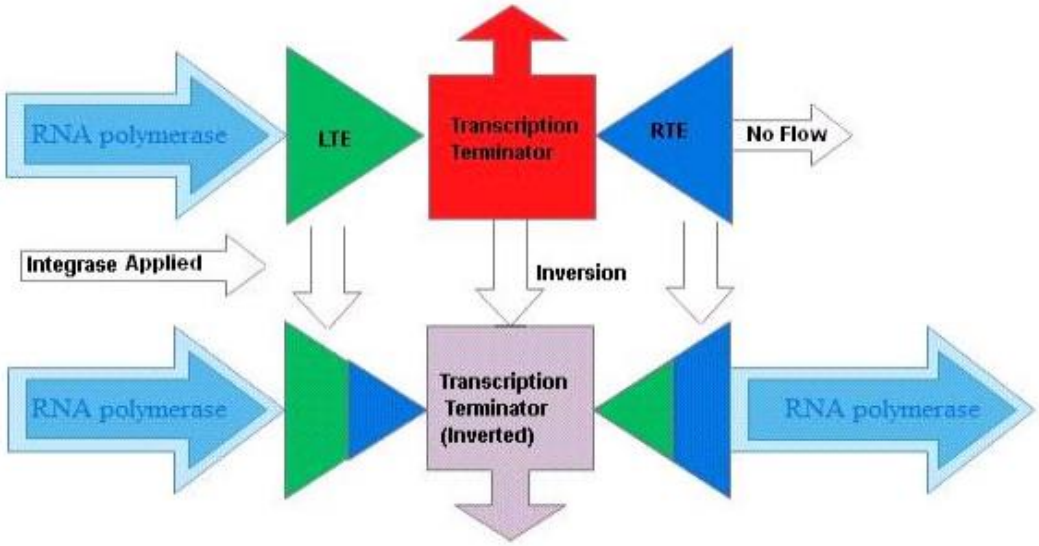



***Fig. 2: Logic Control of RNA Polymerase Flow with Integrase.***

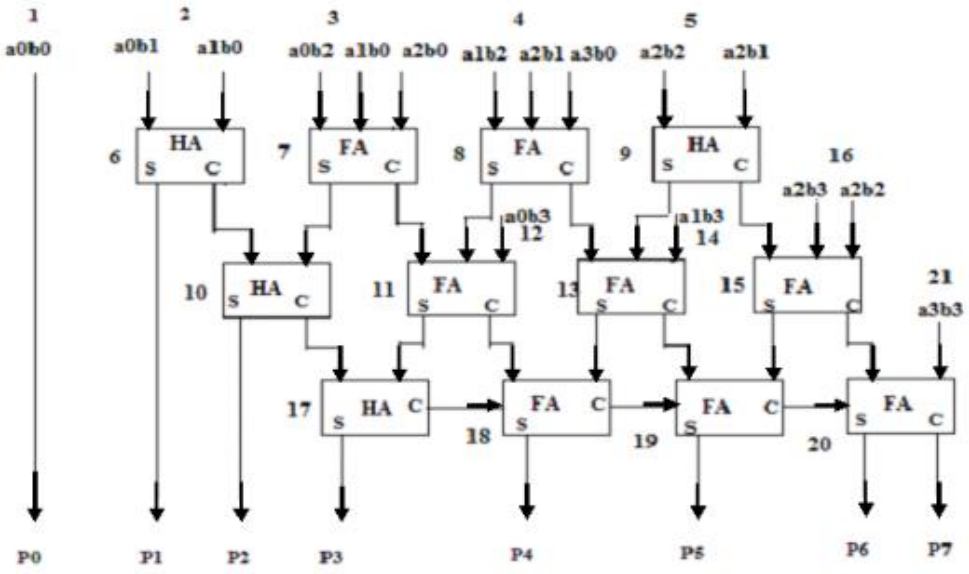



***Fig. 3: Schematic for Wallace Tree Multiplier.***

So, to execute the Wallace tree multiplier design the Full adder and Half adder have to be realized with DNA logic and which can be further decomposed into EXOR, OR and AND gates as shown in Figure 4.


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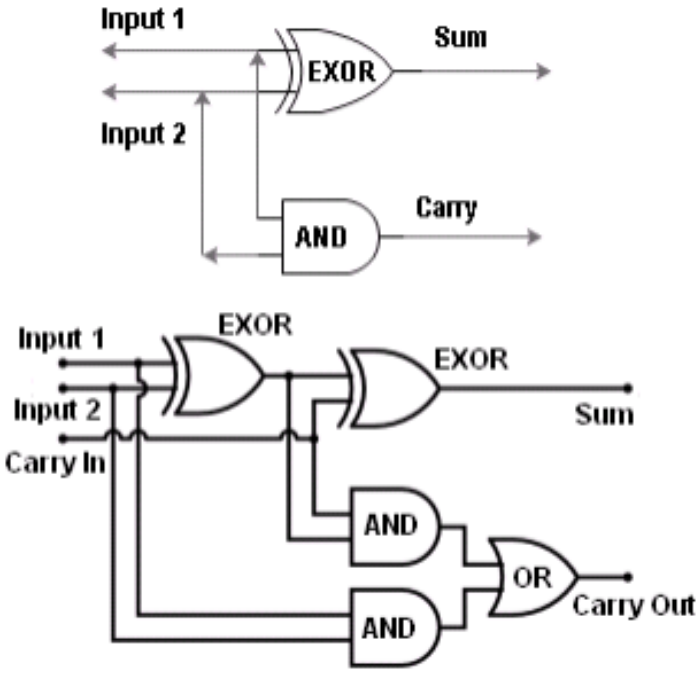



***Fig. 4: Schematic for Logical Half Adder (Top) Full Adder.***

Following few sub-sections have been dedicated to elaborate discussion on those logic gate digital design realizations with DNA logic.

**DNA EXOR LOGIC**

A transcriptor EXOR logic element will be composed off one asymmetric TT with two pairs of TEs recognized by independent integrases. When none of the integrase is present, the terminator will block the transcription as shown in Figure 5.

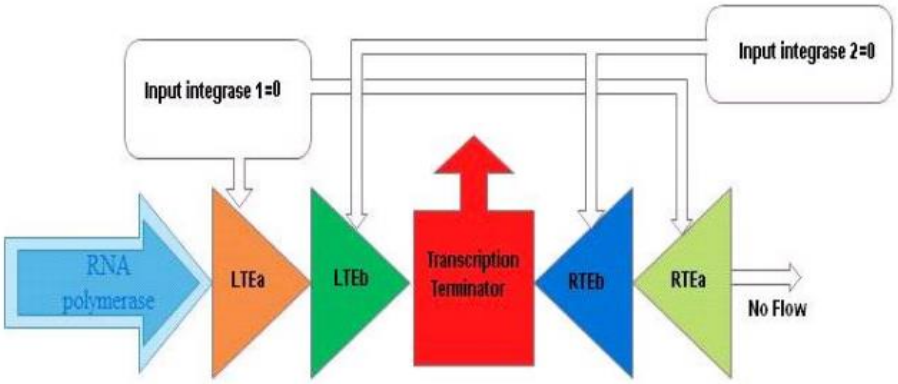



***Fig. 5: Schematic for Logical DNA EXOR showing Blocked Transcription with Absence of Integrase 1 and 2***


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**Symbols:** LTEa and RTEa are associated with integrase 1; LTEb and RTEb are associated with integrase 2, respectively [23].

Presence of any one of the integrase will modify a pair of TE and will flip the TT (by inverting the DNA encoding) which will allow the transcription current to flow ("Figure 6"). Whereas the presence of both the integrases will flip the terminator twice which will restore the terminator"s original orientation and will block transcription again

**DNA AND LOGIC**

A transcriptor AND logic element requires two asymmetric TTs with two pairs of opposing TEs, each associated with each transcription terminator, as shown in Figure 5. The transcription current will flow only when both the intergaces will present but no transcription current flow if only one integrase is present as shown in "Figure 6".

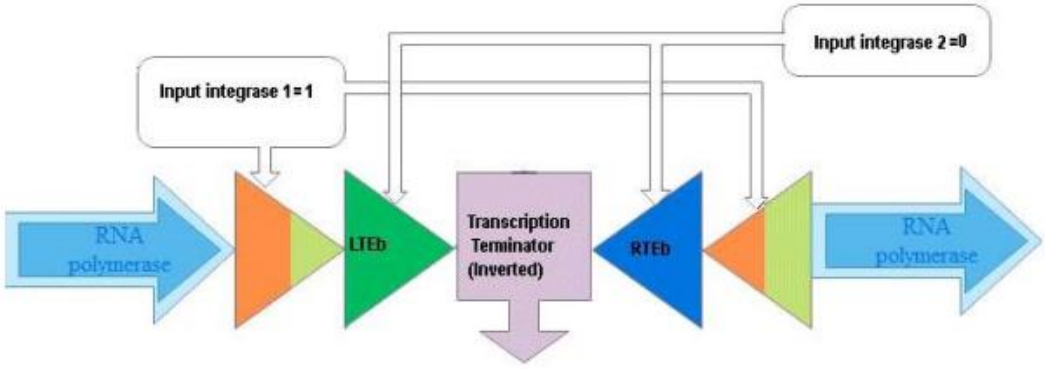



***Fig. 6: Schematic for Logical DNA EXOR showing Transcription Continuation with Presence of Intergace 1 (=1) [23].***

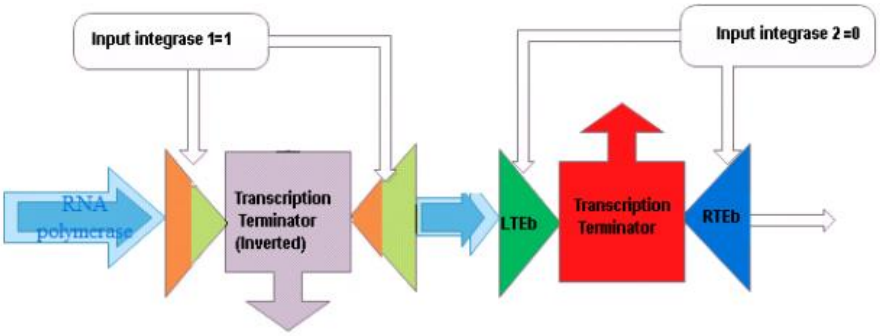



***Fig. 7: Schematic for Logical Representation of AND showing Blocked Transcription with presence of Intergace 1 and Absence of Intergace 2 [23].***


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## DNA OR LOGIC

A transcriptor OR logic element requires only one asymmetric TT with two pairs of favorable TEs associated with TT. Presence of both of the integrases will invert the TT and the current will flow if only one integrase or both of the integrases are absent no current will flow, as shown in "Figure 8"

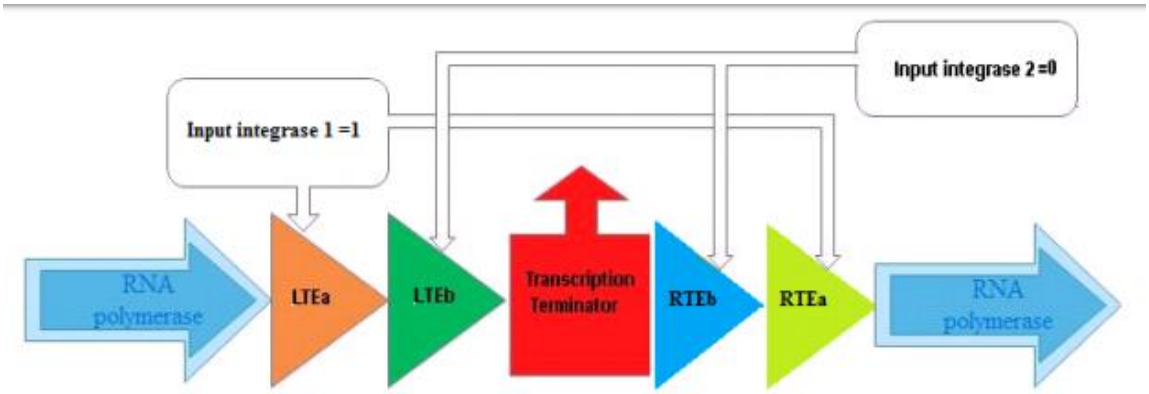



***Fig. 8: Schematic for Logical DNA OR Showing Transcription Continuation with Presence of Intergace 1 (=1) [23].***

With further extension of this concept, other Boolean logics like NAND, NOR, NOT can be also implemented with DNA logic [12–20].

## SIMULATION MODELING

The present 4*4 bit WTM circuit has been logically design and implemented with MATLAB Simulink. The WTM is composed of half adder and full adder subcircuits so the Half adder and Full adder modules have been designed separately with user defined function blocks and the modules have saved in Simulink block library, as shown in Figures 9 and 10, respectively [17].


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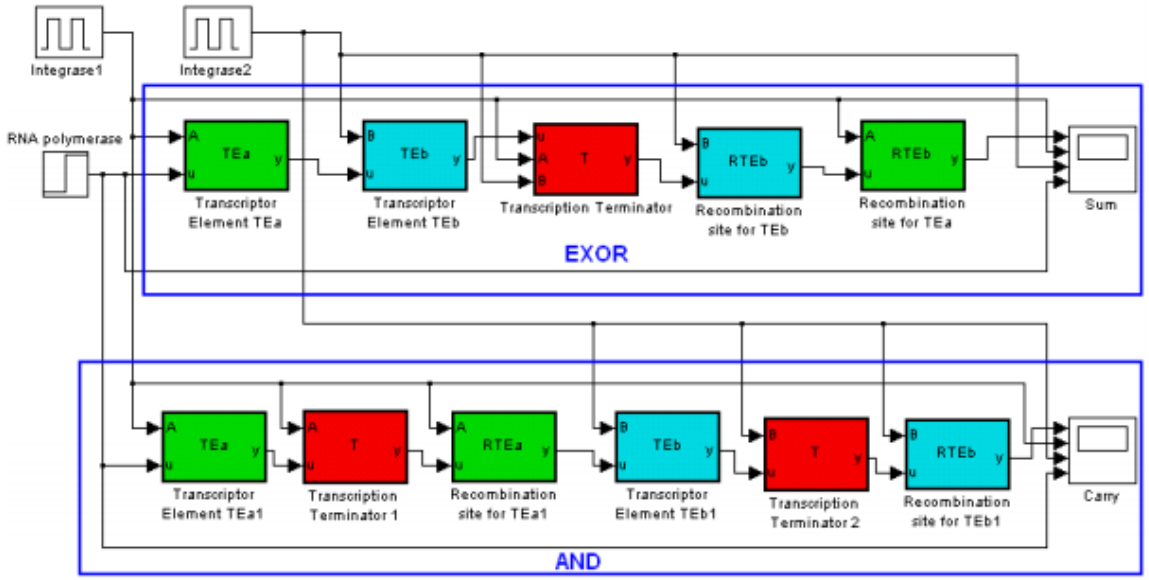



***Fig. 9: Simulink Gate Level Design Of Half Adder; TT: Red Color Block, TEs: Green and Blue Pairs***

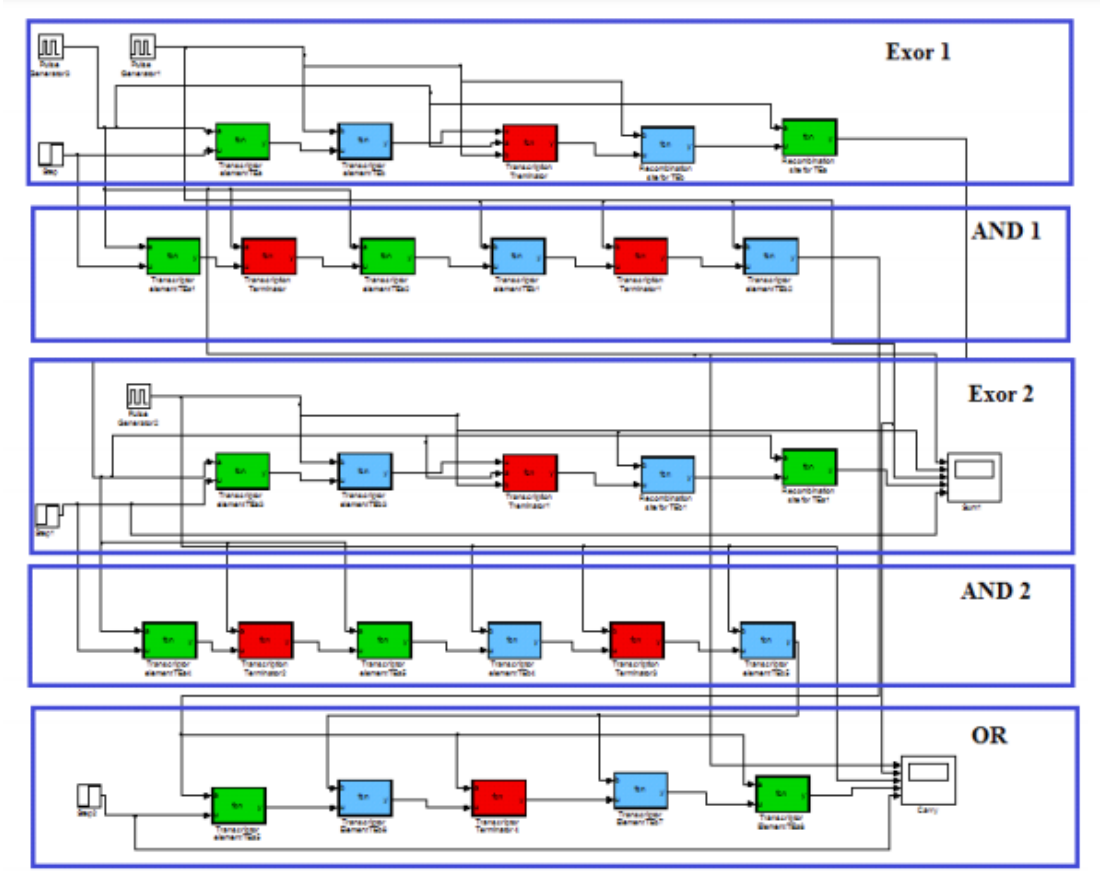



***Fig. 10: Simulink Gate Level Design of Full Adder.***


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The Simulink block diagram of the WTM has been presented in "Figure 11". The RNA polymerase has been considered as input signal and two integrase a, b of 4 bit binary has formed the logic inputs for the Wallace tree multiplier. To implement the Wallace tree multiplier in Simulink user defined function block has been selected from library and every block has been fitted with logical function to replicate transcriptor and transcription elements. Whereas, the pulse source of variable widths have been considered for replicating integrase a, b and a unit step function has been selected to replicate RNA polymerase input.

**Color Symbols:** AND-orange blocks; Half Adder- dark green blocks; Full Adder-light blue blocks; RNA polymerase- Red color block, Integrase a (a0,a1,a2 and a3)-dark blue blocks (top side); Integrase b (b0,b1,b2 and b3): light green blocks (top side).

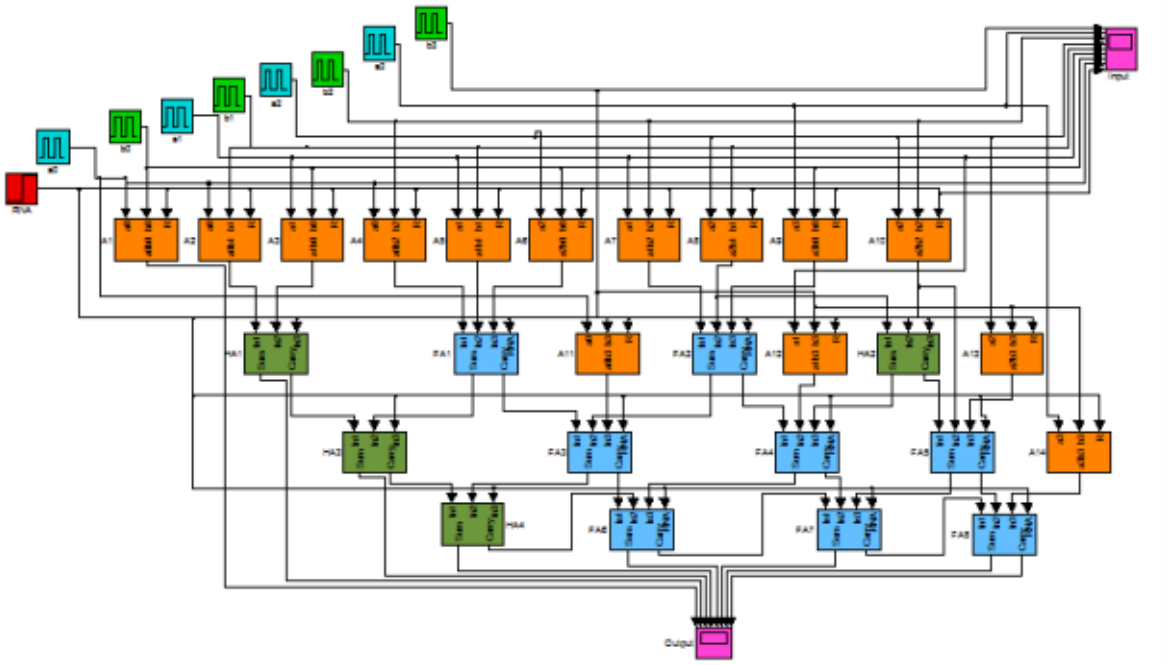


***Fig. 11: Simulink Block Diagram of Wallace Tree Multiplier with 14 and Gates, 4 Half Adders and 8 Full Adders***


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## RESULTS AND DISCUSSION

The proposed WTM simulation model has been designed with MATLAB Simulink software and various digital design aspects like timing diagram, error function, delay factor, area etc. have been theoretically analyzed. Correlation of output with control signal integrase a, integrase b, and input signal (RNA polymerase) has successfully implemented Wallace tree multiplier circuit as shown in "Figures 12 and 13".

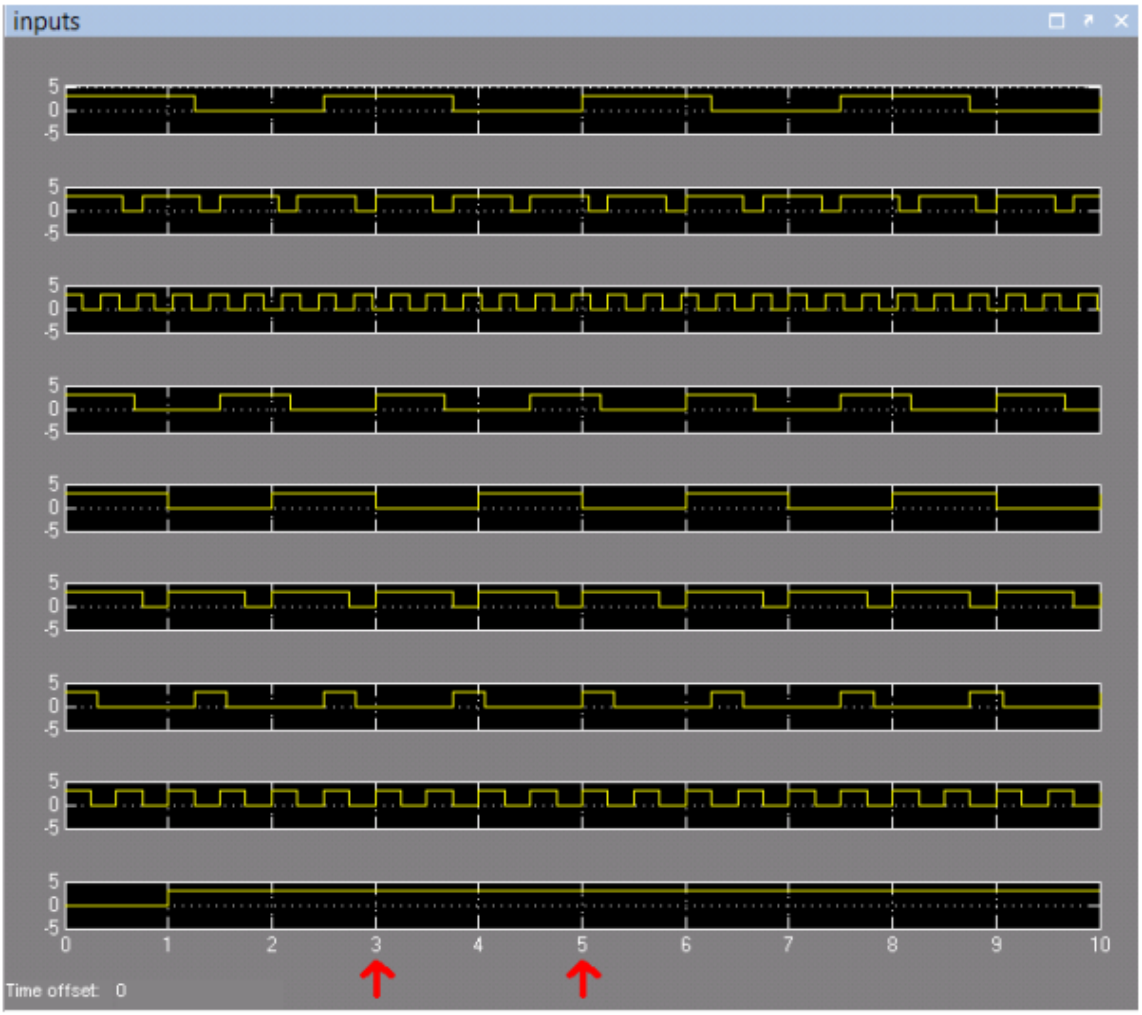



***Fig. 12: With Time the Integrase b3,a3,b2,a2,b1,a1,b0,a0 and RNA Given as Top to Bottom.***


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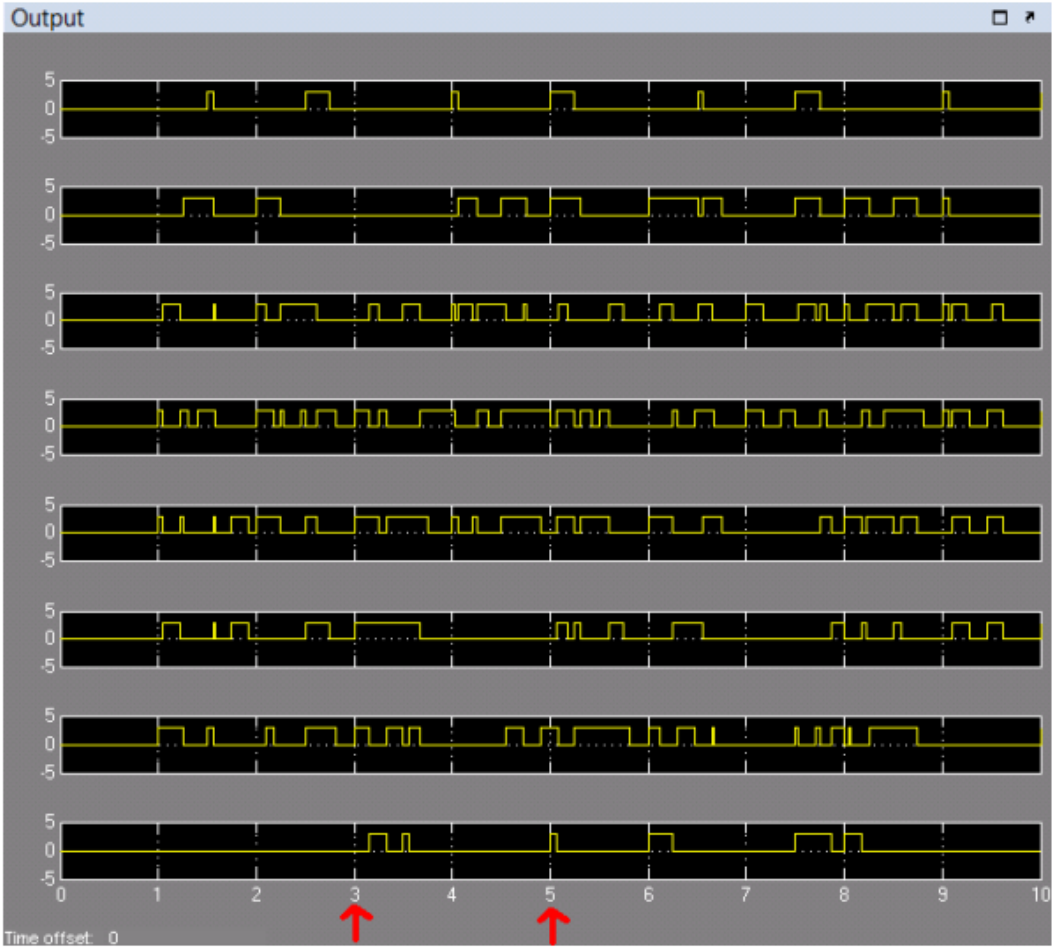



***Fig. 13: With Time the 8 bit Product p7, p6, p5, p4, p3, p2, p1 and p0 Output are Shown from Bottom to Top***

To authenticate the design validity more precisely, correlation between output product terms with integrase a, integrase b, has been presented inform of Truth table at two arbitrary selected time units.

***Table 1: Truth Table for 4*4 bit Wallace Tree Multiplier***

| Time Unit | Integrase a (a3 a2 a1 a0) | Integrase b (b3 b2 b1 b0) | Output Product (p7 p6 p5 p4 p3 p2 p1 p0) |
|---|---|---|---|
| 3 | 1111 | 1000 | 01111000 |
| 5 | 1111 | 1101 | 11000011 |


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A single cell may produce discontinuous responses to small changes in control signals which can be corrected with Population Measurements with n-number of cells. A digitization error rate can be defined as the combined probability of producing false high or low outputs in response to intermediate control signal changes. Based on the experimental analysis presented by Jerome Bonnet et al., the approximated digitization error percentage for AND gate is 10% for input change sequence: 1→0 and 0→1, is 8% for input change sequence: 0→1 and 0→1 and so on [10]. Adopting the same analogy for Half adder the approximated digitization error percentage for sum is 7% for input change sequence: 1→0 and 0→1, is 15% for input change sequence: 0→1 and 0→1 and so on [12]. Based on those experimental results, the digitization error percentages have been calculated for the half adder, full adder design and finally calculated the error percentage for the proposed Wallace tree multiplier design presented in **Table 2**.

Based on the experimental analysis presented by Jerome Bonnet et al. 15-min control-signal pulses were sufficient to activate integrase-mediated switching [12]. So, the each and every gates present in the circuit will require 15 min for their switching. For half adder and full adder the every possible input-output path has been identified and longest path in terms of maximum number of logic gate has been considered to estimate the maximum delay. For the half adder the maximum delay or maximum switching time has been calculated as 15 min whereas in the full adder it is 45 min. Similarly for WTM, the delay for each possible path is given in Table 3, from that the maximum propagation delay for the proposed Wallace tree multiplier is calculated as 4 hours.

***Table 2: Error Percentage Table for Wallace Tree Multiplier.***

| Change in time unit | Integrase a (a3, a2 ,a1, a0) | Integrase b (b3, b2, b1, b0) | Change in output p (p7, p6, p5, p4, p3, p2, p1, p0) | Sum (error in %) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | P7 | p6 | p5 | p4 | p3 | p2 | p1 | p0 |
| 3 | 0→1,0→1, 0→1,0→1 | 1→1,0→0, 1→0,0→0 | 01111000 | | 10 | 10 | 10 | 7 | | | 2 |
| 5 | 1→1,1→1, 0→1,0→1 | 0→1,1→1, 1→0,0→1 | 11000011 | 25 | 7 | 15 | 7 | | | 7 | 8 |


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***Table 3: Delay Table for the Wallace Tree Multiplier Circuit.***

| Sl no. | Possible paths from input to output P (delay calculated) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | p0 | p1 | p2 | p3 | p4 | p5 | p6 | p7 |
| 1 | 1 (15 min) | 2-6 (30 min) | 2-6-10 (45 min) | 2-6-10-17 (1hr 15min) | 3-7-11-17-18 (2hr 45min) | 4-8-11-18-19 (3hr 15min) | 4-8-11-18-19-20 (4hr) | 4-8-11-18-19-20 (4hr) |
| 2 | | | 3-7-10 (1hr 15min) | 3-7-11-17 (2hr) | 4-8-11-18 (2hr 30min) | 4-8-13-19 (2hr 30min) | 5-9-15-20 (2hr) | 5-9-15-20 (2hr) |
| 3 | | | | | 4-8-13-18 (2hr 30min) | 5-9-14-13-19 (2hr) | 21-20 (1hr) | 21-20 (1hr) |
| 4 | | | | | | 5-9-15-19 (2hr ) | | |
| 5 | Total propagation delay for the Wallace tree multiplier is | | | | | | | 4hr |

It is quite clear from the present analysis that proposed DNA based WTM will give significant advantage over conventional silicon based WTM mainly in terms of area and power whereas as the delay factor and error will be considerably in higher side. But that factor can be significantly eradicated with advancement of bioelectronic device design technology in coming future. Also, development of proper mathematical model of DNA transistors in coming future will open up analog modeling option and will provide more accurate analysis of DNA based logic circuit.

## CONCLUSION

Under the present work the DNA logic gate design concepts has been theoretically investigated in detail. The logical design concepts of EXOR, AND and OR gate have been implemented with proper understanding and explanations. Finally a 4*4 bit Wallace tree multiplier has been logically designed with DNA based AND, Half adder and Full adder circuit with MATLAB Simulink model. The timing diagrams for the multiplied output, logic inputs and input signal are simulated. The digitization error in percentage has also been approximated and presented for different input combinations for the WTM circuit. And, also the propagation delay for WTM circuit is calculated and presented for all possible paths between inputs to output. Such block level design of DNA WTM circuit will provide valuable understanding about the technological advantages of DNA based logic circuit design. Not only that such block level design can be added with proper mathematical model of DNA transistor which will initiate the development of future bioelectronics circuit simulators.


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