MANTECH Publications

Journal of Research in Electrical Circuits and Systems
Volume 7, Issue 3, September-December 2022

New Active Body-Based Doind-ABC2 for High-Speed Domino Logic at the 70nm Node Technology

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Abstract

In current VLSI technology, high speed devices are employed in many applications, such as dynamic logic circuits, since they outperform static devices in terms of latency, noise immunity, and power consumption. Increased leakage current combined with noise immunity degrades dynamic logic circuit performance.

The body biassed DOIND-ABC2 (DOIND-2) logic is introduced in this study to decrease leakage current with reduced delay cost. In this study, a distinct Active body biassed strategy for DOIND logic approach, termed DOIND-2(ABC-2), was applied to examine various parameters. The suggested DOIND-2 strategy provides a maximum 70 percent reduction in leakage current when compared to the Domino, DOIND, and DOIND-1 proposed techniques. The proposed DOIND-2 strategy also outperforms all existing approaches in the majority of parameters. The influence of frequency fluctuation in various circuits has been studied in this work. All parameters were tested at the 70 nm technology node with the Tanner EDA tool and a supply voltage of 0.9v.

Keywords: *DOIND-2, Valuation, Power dissipation, bias in the active body Domino logic*

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INTRODUCTION

The introduction of performance boosters such as novel materials and innovative device structures has become necessary for the future of CMOS scaling in the VLSI industry.

Improved portable system performance and lower power consumption in extremely high density VLSI chips result in rapid and imaginative evolution of low power design. Higher power decay affects battery life and dependability in battery-powered applications. The leaking with each new technological breakthrough, current grows dramatically. Leakage power loss is a key issue in deep-submicron technologies since it drains the battery even when a system (Circuit) is entirely inactive. The power supply voltage and threshold voltage of MOS transistors are key factors for regulating the performance and switching speed of MOS devices as the technology node is scaled down. The domino logic Active Body Biased DOIND-ABC2 (DOIND-2) Approach is utilised in this work to assess various parameters.

RELATED WORK

VLSI technology employs many approaches to control leakage current in domino logic circuits. Some techniques for controlling leakage current are discussed.

Two leakage control transistors (one PMOS and one NMOS) are introduced between pull-up and pull-down circuits within typical logic circuits in the Lector Technique. This configuration assures that one of the LCTs is always operating in the vicinity of its cut off area. The LECTOR method is based on the concept of "a condition with more than one transistor OFF along a circuit from supply voltage to ground."

The INDEP approach is a method for reducing leakage current in nanoscale circuits. Extra inserted transistors between pull up and pull down networks that are input logic dependent are used in this strategy.

DOIND method [6] DOIND logic circuit (Domino logic with Clock and INput Dependent transistors). It has two DOIND transistors linked between A and B, MP4 (PMOS) and MN4 (NMOS). DOIND transistors' gate terminals (MP4 and MN4) are V0 and V1, which are clock and input logic dependent, respectively.

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PROPOSED WORK

Adopting body biasing DOIND logic

DOINDAB (Domino logic with Clock and INput Dependent transistor with Active Body Biasing) ABC2 was proposed in this work. The body of the static circuit is made up of SOI partly depleted MOSFETs that are biassed to regulate the threshold dynamically.

DOIND-2 (ABC-2) Technique

Figure 1.1 depicts a suggested DOIND-2 logic circuit. It has two DOIND transistors linked between A and B, MP4 (PMOS) and MN4 (NMOS). DOIND transistors' gate terminals (MP4 and MN4) are V0 and V1, which are clock and input logic dependent, respectively. The body biassing MP5 (PMOS) has been installed in the transistor MP4 (PMOS). PMOS transistor MP5's gate terminal is linked to the gate terminal of PMOS transistor MP4, and its source terminal is connected to the point A of PMOS transistors MP1 and MP4. The Drain terminal of PMOS transistor MP5 is linked to the Body terminal of PMOS transistor MP4. Set the Body Biasing MN5 (NMOS) to the Transistor MN4 (CMOS).

MN5 NMOS transistor is biassed by MN4 NMOS transistor. The gate terminal of the NMOS transistor is linked to the gate termina1 of the NMOS transistor MN4, the source is attached to the Body terminal of the NMOS transistor MN4, and the drain terminal is connected to point B of the NMOS transistors MN2 and MN4. All PMOS transistors have their body terminals linked to Vdd, while all NMOS transistors have their body terminals connected to Gnd.

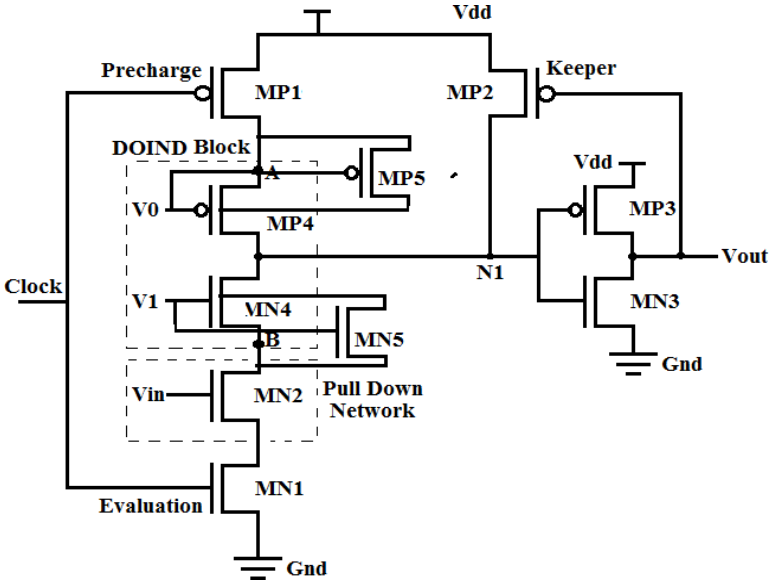


Fig: 1.1: DOIND-2 Logic circuit

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The DOIND-2 logic circuit operates in the following manner. When the clock signal is low, V0 should be 0 (low), allowing MP1, MP4, and MP5 to switch on and the DOIND logic circuit to enter the precharge phase. During the precharge phase, node N1 is charged to Vdd through MP1, MP4, and MP5. The circuit's Vout is low, causing the keeper transistor to switch on (MP2). The circuit begins the evaluation phase when the clock signal is high. In the evaluation phase, when input Vin = 1 (high), V1 should be 1, and when input Vin = 0 (low), V1 should be 0, such that dynamic node N1 becomes 1.

Different parameter analysis of Adaptive Body biased DOIND approach

The TSPICE simulator is used in this part to explore DOMINO logic-based buffers with varying clock frequencies. All experimental data were collected at the 70nm technology node. Except for the keeper transistor, the channel width and length of NMOS transistors are the same at 270ns while channel length of PMOS transistors are 2X of channel length. The keeper transistor's channel length is 5X and its width is 2X of the technology node. For the simulation, the Vdd power source is set at 0.9 volts.

Because the circuit's latency and leakage current are functions of the clock pulse, input value, and logic circuits.

Impact on Leakage Current:

Relation between leakage current and threshold voltage is given by [6],

$$I_{Leakage} = I_0 \frac{(Vgs-Vth)}{\eta Vt}(1-\exp\frac{-Vd}{Vt})$$

Where Vgs is gate to source voltage; I0 is saturation current, and η is subthreshold slope factor and Vt is drain to source voltage.

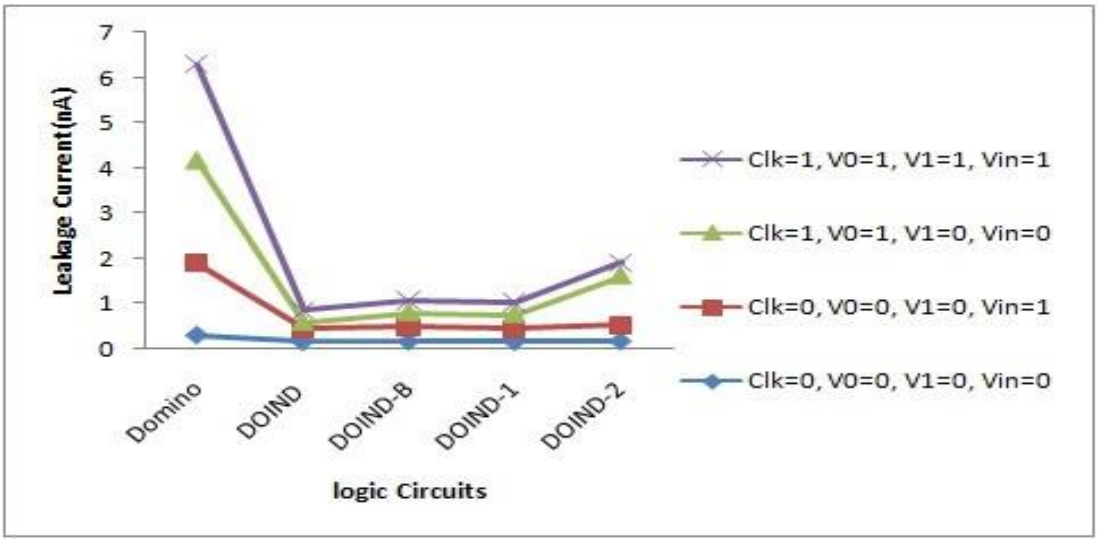
Table:1: Leakage current at different clock pulse.

logic design	Clk=0, Vin=0	Clk=0, Vin=1	Clk=1 Vin=0	Clk=1, Vin=1	Improv In %
Domino	0.307	1.595	2.262	2.126	
DOIND	0.160	0.307	0.127	0.258	86%
DOIND-B	0.166	0.322	0.322	0.264	83%
DOIND-1	0.160	0.307	0.306	0.259	84%
DOIND-2	0.175	0.358	1.091	0.278	70%

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DOIND -2 have 70% better improve than the Standard Domino logic but DOIND indicate the best result 86% improvement than other comparative logic circuits.

At the clock $=V_1=V_{IN}=0$ show the lower leakage current at all the logic circuits but when we apply clock $=V_1=V_{IN=}1$ all the logic have higher leakage current.



Impact on Static Power:

Static Power defined by the given formula.

Static Power = Leakage Current*Vdd, Where Vdd is the power supply of the logic Circuits.

Table2: Impact on Static Power

logic design	Clk=0 Vin=0	Clk=0 Vin=1	Clk=1Vin=0	Clk=1 Vin=1	% improv
Domino	0.276	1.435	2.036	1.913	
DOIND	0.144	0.276	0.115	0.232	86%
DOIND-B	0.149	0.290	0.290	0.237	83%
DOIND-1	0.144	0.276	0.276	0.233	84%
DOIND-2	0.157	0.322	0.982	0.250	70%

From the above table DOIND, 86% improvement than domino logic circuit But DOIND-2 have also 70% better than the Domino Logic circuit.

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Impact on Static Energy:

Static energy element is directly proportional to Vdd so static energy is represented as

$$E_{Static} = I_{Leakage} V_{dd} T_{delay}$$

Where $I_{Leakage}$ is leakage current and T_{delay} is circuit delay.

Table: 3: Static Energy at different clock frequency

logic design	At 50MHz	Gain	At 5MHz	Gain
Domino	92.971		158.10	
DOIND	19.132	79%	19.709	88%
DOIND-B	36.400	61%	33.408	79%
DOIND-1	57.194	38%	2.5085	98%
DOIND-2	39.807	57%	65.125	59%
logic design	At 500kHz	Gain	At 50kHz	Gain
Domino	158.1		155.70	
DOIND	20.08	87%	20.094	87%
DOIND-B	30.78	81%	30.880	80%
DOIND-1	2.478	98%	4.653	97%
DOIND-2	59.98	62%	58.26	63%

Static Energy Gain is lower at higher frequencies, yet it outperforms Domino Logic by 57 percent, 59 percent, 62 percent, and 63 percent. The table demonstrates that decreasing the clock frequency yields the greatest benefit.

Impact on Static PDP

Static energy delay product (EDP) and Static power delay product (PDP) is given by

$$EDP_{static} = E_{static} \times T_{delay}$$

$$PDP_{static} = P_{static} \times T_{delay}$$

Table 4. shows various logic circuits and there value of static PDP with different clock frequency.

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Table: 4.: Static PDP on different clock periods

Logic design	50MHZ	% impro	5MHZ	% impro
Domino	92.97		158.1068	
DOIND	19.13	79%	19.70967	88%
DOIND-B	33.36	64%	33.40882	79%
DOIND-1	62.64	33%	2.747437	98%
DOIND-2	39.80	57%	65.12519	59%
Logic design	500KHZ	% impro v	50MHZ	% impro v
Domino	158.10		155.7074	
DOIND	20.075	87%	20.09425	87%
DOIND-B	30.780	81%	30.88084	80%
DOIND-1	2.7143	98%	5.097285	97%
DOIND-2	59.979	62%	58.26607	63%

Static PDP shows around the same improvement as Domino Logic circuit. When we raise the clock frequency, the improvement decreases.

Impact on Dynamic power:

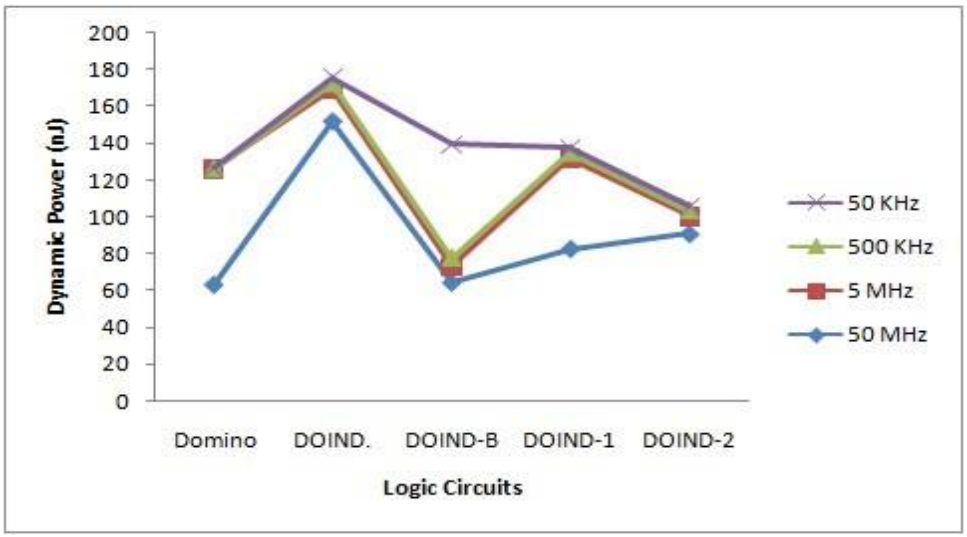
Power consumed when the inputs are active is referred to as dynamic power. When inputs are active, capacitances charge and discharge, and power rises as a result. The dynamic power comprises both the alternating current component and the static component.

Table: 5: Dynamic Power at different frequency

Logic design	50MHZ	% improve	5MHZ	% improv
Domino	63.10273		63.10273	
DOIND.	151.7647	-141%	17.3993	72%
DOIND-B	64.24351	-181%	8.995963	86%
DOIND-1	82.51929	-31%	49.50935	22%
DOIND-2	90.62208	-44%	9.847387	84%
Logic design	500KHZ	% improve	50KHZ	% improv
Domino	0.111690		0.11	
DOIND.	3.702617	-3215%	2.493134	-2166%
DOIND-B	4.287091	-3738%	61.87233	-5614%
DOIND-1	3.004553	-2590%	2.423472	-2103%
DOIND-2	3.189672	-2756%	2.461738	-2138%

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Table shows that clock frequencies of 50MHz, 500KHz, and 50KHz Dynamic Power have drawbacks, but at 5MHz, DOIND, DOIND-B, DOIND-1, and DOIND-2 (ABC2) exhibit 72 percent, 86 percent, 22 percent, and 84 percent improvement over Domino Logic circuit.



Impact on Delay:

When it comes to speed, most designs will include multiple logic routes that do not involve any conscious effort. However, there will generally be a number of crucial pathways that demand attention to timing specifics. These can be identified by experience or timing simulation, but most designers utilise a timing analyzer, which is a design tool that discovers the slowest pathways in a logic architecture automatically.

Table; 6: Delay at different clock period

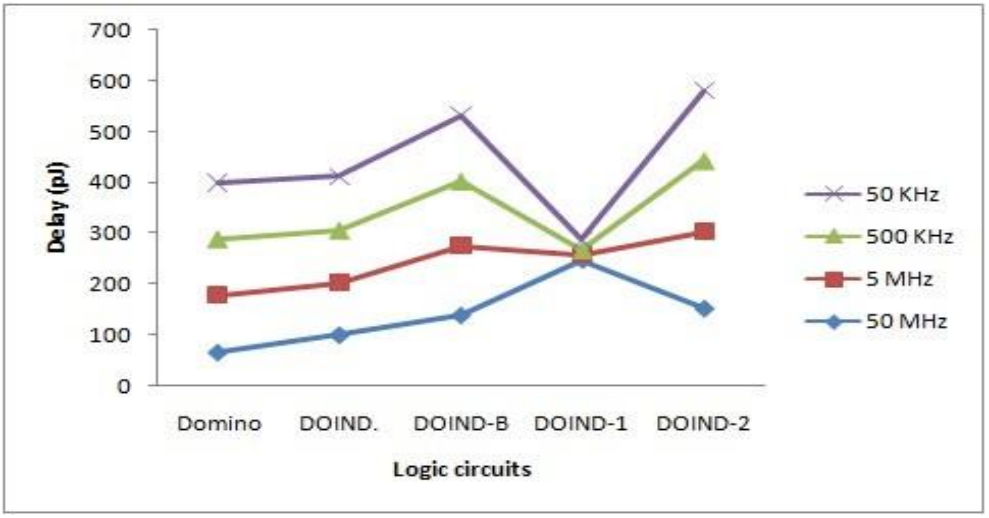
Logic design	500KHZ	% improv	50KHZ	% improve
Domino	111.6905		110	
DOIND.	104.4	7%	104.5	5%
DOIND-B	127.1756	-14%	127.59	-16%
DOIND-1	10.65	90%	20	82%
DOIND-2	140	-25%	136	-24%

DOIND-2 demonstrates the disadvantages here. However, DOIND and DOIND-1clear outperform Domino logic circuits by 8% and 90%, respectively.

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Table; 7: Delay at different clock period

Logic design	50MHZ	% improv	5MHZ	% improve
Domino	65.68		111.69	
DOIND.	99.5	-51%	102.5	8%
DOIND-B	137.87	-110%	138.03	-24%
DOIND-1	245.78	-274%	10.78	90%
DOIND-2	151.06	-130%	152.01	-36%



Impact on Dynamic PDP:

The table demonstrates that DOIND-2 outperforms Domino Logic by 79 percent at the 5MHZ, 500KHZ, and 50KHz frequencies. DOIND-2 logic improves around 92 percent and 95 percent more than Domino logic, while DOIND, DOIND-B, and DOIND-1 also outperform Domino logic circuits for these two clock frequencies.

Table: 8: Dynamic PDP at different clock period

Logic design	**50MHZ**	**% improv**	**5MHZ**	**% improve**
Domino	4.144		7.0482	
DOIND.	15.10	-264%	1.7834	75%
DOIND-B	8.857	-114%	1.2417	82%
DOIND-1	20.28	-389%	0.5337	92%

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DOIND-2	13.68	-230%	1.4969	79%
Logic design	**500KHZ**	**% improve**	**50KHZ**	**% improve**
Domino	7.047		6.9413	
DOIND.	0.386	95%	0.2605	96%
DOIND-B	0.545	92%	7.8944	-14%
DOIND-1	0.031	100%	0.0484	99%
DOIND-2	0.446	94%	0.3347	95%

SIMULATION RESULT

In this work, all of the parameters for domino logic, DOIND, DOIND-B, DOIND-1, and DOIND-2 approaches are examined with the EDA tanner at 0.9V supply voltage. The TSPICE simulator is used in this part to explore DOMINO logic-based buffers with varying clock frequencies. All experimental data were collected at the 70nm technology node. Channel width= channel length =270ns for NMOS transistors, while channel width of all PMOS transistors except the keeper transistor is 2X of channel length. The keeper transistor's channel length is 5X and its width is 2X of the technology node.

CONCLUSION AND FUTURE SCOPE

Leakage power dissipation is a fundamental problem in VLSI design. Leakage current reduces the performance of a portable device's battery. Even when the circuit is in the idle and reset states. Without running the item, unnecessary power consumption is maintained. This chapter discusses the work's contribution and the technology's future potential.

This paper effort focuses mostly on several adoptive body biassed technologies for the DOIND method. Among all other circuits, the proposed DOIND-2 exhibits a 70% reduction in leakage current. All of the circuits were tested at four different clock frequencies: 50MHz, 5MHz, 500 KHz, and 50 KHz. We utilise the 70nm technology node to analyse the circuits here, however other node technologies may be used.

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