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Investigation of the Behavior of Subthreshold Circuits in Response to Changing Temperatures

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Abstract

Due to the explosive growth of battery-less electronics and biomedical applications, ultra-low-power (ULP) circuits have drawn a lot of attention. ULP circuits employ the subthreshold region of transistor operation. The primary research challenge in the subthreshold operating region is to reap the benefits of ULP while suffering the least amount of speed and robustness loss. The performance of subthreshold circuits is significantly impacted by variations in Process, Voltage, and Temperature (PVT). Temperature changes have the potential to significantly alter the designed performance parameters of ULP circuits. The purpose of this paper is to determine the impact of temperature variation on device and circuit performance parameters at various biassing voltages in the subthreshold region. According to simulation results, performance parameters are significantly impacted by deep subthreshold and near threshold voltage regions, whereas moderate subthreshold voltage regions are where subthreshold circuits are more resistant to temperature changes. This proves that temperature immune circuits work best in the moderate subthreshold region.

Keywords: *Subthreshold, ultralow power, temperature variations.*

INTRODUCTION

In 1965, Gordon E. Moore predicted that the functionality per chip would increase as the number of transistors per chip roughly doubled every two years [1]. This trend is made possible by technology

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scaling, which improves the speed of logic gates to support higher clock frequencies and lower energy consumption per operation. Even though the energy required for each operation has decreased, the total amount of power consumed by each chip has increased significantly [2]. Moore's law is satisfied by accelerated technological scaling that prioritises high performance while making power dissipation a secondary design concern. By increasing chip size and/or evolving device scaling, the maximum number of devices on a chip has significantly increased. This causes self-heating, increased dynamic/leakage power dissipation, and decreased device robustness. However, due to a significant increase in the demand for portable and biomedical applications over the past ten years, as well as an increase in both dynamic and leakage power dissipation, power dissipation has gradually become a crucial design issue, with speed as a secondary design criterion. For the highest performing circuits, increased power dissipation in the nanometer regime may be tolerable. However, for intended ULP applications, it is the most difficult design problem. The growing power issue has been addressed in a number of ways [3–6], but in order to achieve ULP consumption, a transistor must operate in the subthreshold region [7].

Fig. 1 shows different energy consumption components as a function of supply voltage. It is clear from Fig. 1 that minimum energy operation can be obtained only under subthreshold conditions. To fulfill ULP demand of portable biomedical applications, research community has shifted their focus towards subthreshold operating region [8-10]. Device operating in subthreshold regime has shown strong potential towards satisfying the ULP requirements of moderate throughput portable systems.

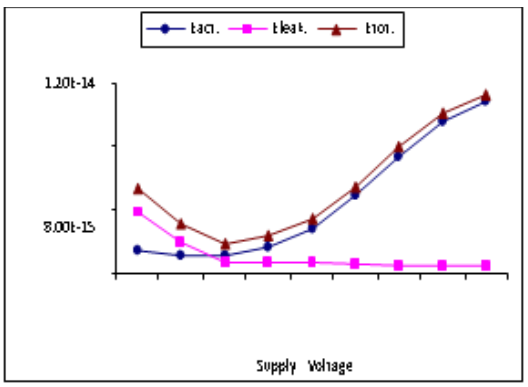


Fig. 1 Energy as a function of Supply Voltag

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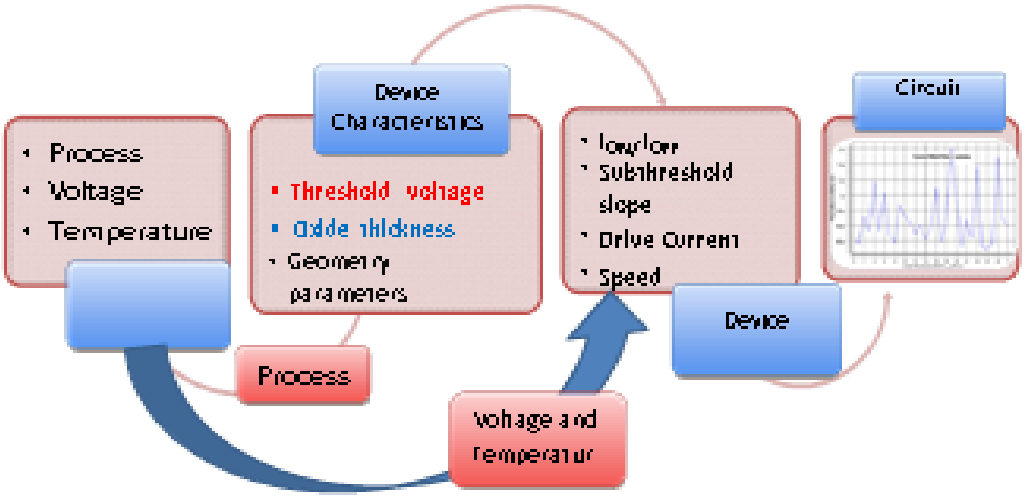


Fig. 2 Effect of PVT variation on device and circuit performance metrics

To achieve ULP levels, the supply voltage (VDD) must be scaled below the device's threshold voltage (Vth), which presents design challenges for enhancing circuit delay and robustness [10–12]. As shown in Fig. 2, variations in PVT parameters have a significant impact on subthreshold circuit performance and can result in these circuits malfunctioning.

Subthreshold circuits' field of application will grow as their speed and robustness increase. This paper primarily contributes to the investigation of temperature variations under subthreshold conditions that affect device and circuit performance parameters. It proves that temperature-sensitive immune circuits are drawn to the moderate subthreshold region. The remainder of this essay is structured as follows: The subthreshold region of MOSFET operation is examined in Section II. The impact of temperature variation on device and circuit performance parameters is examined in Section III. Section IV then brings this essay to a close.

Sub threshold Region of Operation

The demand for battery-operated mobile platforms and new technologies like body area networks, RFIDs, biomedical devices, cell phones, and distributed sensor networks has increased over the past few years. These technologies also have lower power budgets for ultra-low energy operation as opposed to higher performance. The challenging design challenge in such applications is to maximise operational life by minimising power dissipation. ULP demand for portable devices is satisfied by operating devices in the subthreshold region. The sub-threshold leakage current (Vgs<Vth), which is caused by the diffusion of

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minority carriers in a non-conducting transistor, is the most significant leakage current for ultra-low power applications. Under these circumstances, the transistor is functioning in a weak inversion region.

On the channel's surface, the minority carriers flow as a result of the potential applied between the drain and source. These underrepresented carriers are employed as switchers. Equation (1), which is given in Fig. 3 [5], describes how a MOSFET's subthreshold leakage current changes exponentially with temperature, gate voltage, and threshold voltage.

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th}+\eta V_{DS})}{nV_T}} (1-e^{\frac{-V_{DS}}{V_T}})$$

where I_0 is given by,

$$I_0 = \mu_0 C_{ox} \frac{vv}{I} (n-1)V_T^2$$

Where V_{th} is the transistor threshold voltage, n is subthreshold slope factor ($n=1+C_d/C_{ox}$), V_T is the thermal voltage, isDIBL coefficient. V_{th} is given by equation (3) [12].

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$$V_{th} = V_{FB} + (\Phi_{S0} - \Lambda\Phi_S) + \gamma \sqrt{\Phi_{S0} - V_{bs}} \left(1 - \lambda \frac{Xd}{L_{eff}}\right) + \Delta_{VNWE} \quad (3)$$

Where, V_{FB} is the flat-band voltage, Φ_{S0} is zero bias surface potential, is the body factor, X_d is the depletion layer thickness.

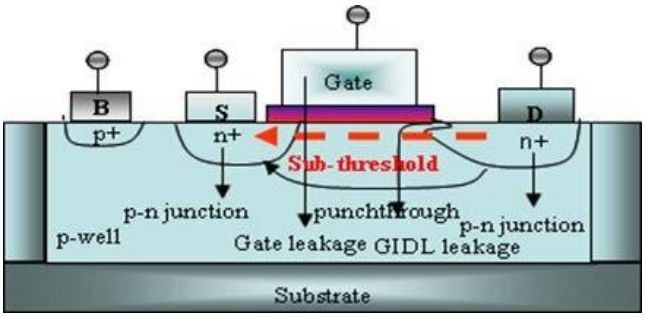


Fig. 3 Leakage components in a MOSFET

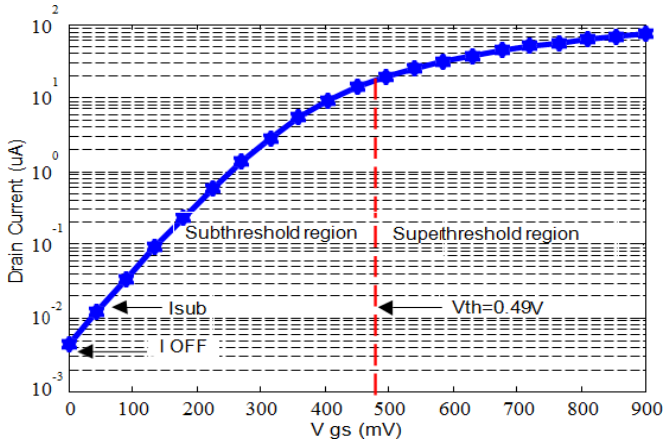


Fig. 4 I-V characteristics of Si-MOSFET

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The elements of a Si-leakage MOSFET's current are depicted in Fig. 3. Subthreshold current flowing in a weakly inverted channel from drain to source is the useful component. Due to the flow of carriers through diffusion, subthreshold current has an exponential dependence on the gate-to-source voltage (VGS), as shown in Fig. 4. Subthreshold leakage current increases exponentially as temperature rises because it lowers the threshold voltage.

Effect of Temperature Variation on Subthreshold Circuit Performance

To maintain speed and reduce energy consumption, elegant scaling requirements on VDD and Vth present a number of technological and circuit design challenges. The two main design issues in advanced above threshold nanoscale CMOS technology are static leakage and variability issues, even though technology scaling has reached the required speed. PVT variations are, however, of great interest when designing robust ULP systems along with speed because of the subthreshold drive current's exponential dependence on Vth, VDS, and temperature in the subthreshold operating region. The impact of temperature variation on subthreshold circuit performance is examined in this section. Subthreshold current I sub increases exponentially with temperature, in contrast to superthreshold, where mobility predominates due to highgate overdrive and transistors' drain current ION decreases as temperature rises [13]. It is necessary to research the impact of temperature variation under subthreshold regime at various biassing conditions. Equation (1) is represented by [14].

$$Isub = \mu_0 C_{ox} \frac{W}{L} (n-1) \frac{K^2}{q^2} \frac{(V - V)}{n(kT)} \left[1 - e^{-V_{DS}} \right] \quad (4)$$

The direct temperature dependence of Isub is demonstrated by equation (4). Based on HSPICE simulations using 32nm technology node PTM files, this section makes several significant observations about the temperature dependence of subthreshold leakage current and various device parameters. All measurements are made for the third inverter in a chain of five stage inverters, which is used as a test bench.

For various gate overdrive voltages, Fig. 5 illustrates the impact of temperature variation on drain current in subthreshold conditions. From Fig. 5, it can be seen that Isub rises as temperature rises below 350 mV VDD. The impact of temperature variation on Isub is minimal at 350 mV VDD. Above this voltage, Isub rises as the

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temperature rises. Therefore, it can be concluded that the gate-overdrive voltage affects how quickly Isub changes. The impact of temperature variation on device trans conductance at various biassing voltages is depicted in Fig. 6.It has been observed from Fig. 6 that in deep subthreshold region (VDD=0.2V), the trans conductance increases with temperature. As supply voltage increases, trans conductance decreases with temperature especially in moderate subthreshold region and in superthreshold region due to the decrease in drive current as shown in Fig. 6. At VDD = 0.3V, the temperature effect on trans conductance is minimum.ION/IOFF mainly determines the power dissipation of the device. ION is the subthreshold leakage current at VDD=VGS=VDS and IOFF is the leakage current at VGS=0V and VDS=VDD. For better performance, higher ION/IOFF is preferred. Figure 7 shows the effect of increase in temperature on ION/IOFF ratio. As temperature increases, ION/IOFF ratio decreases significantly. This is due to higher rate of change of IOFF with respect to. temperature compared to ION. Though drive current increases with rise in temperature, device OFF current also increases which results in higher leakage power dissipation. Fig. 8 shows that with the increase in temperature, threshold voltage decreases. It has also been observed that with the increase in supply voltage, threshold voltage decreases significantly. Increasing temperature from 20°C to 120°C decreases Vth by 7.78%, 8.88% and 13.26% for VDD=0.2V, 0.4V and 0.9V respectively.

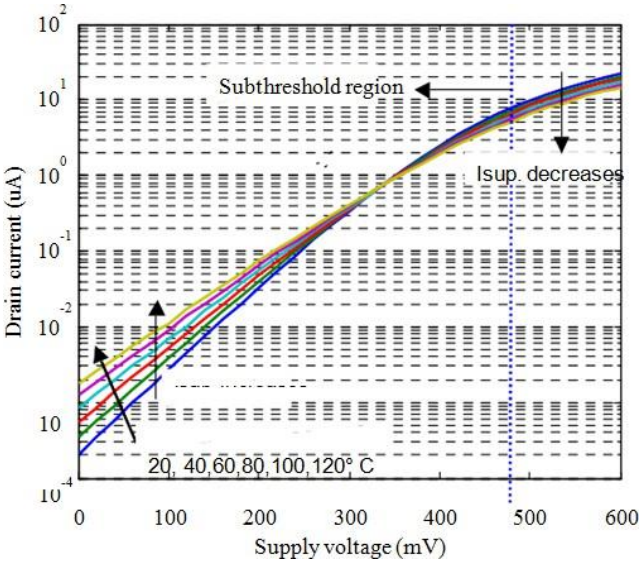


Fig. 5 I-V characteristics of Si- MOSFET at different temperatures

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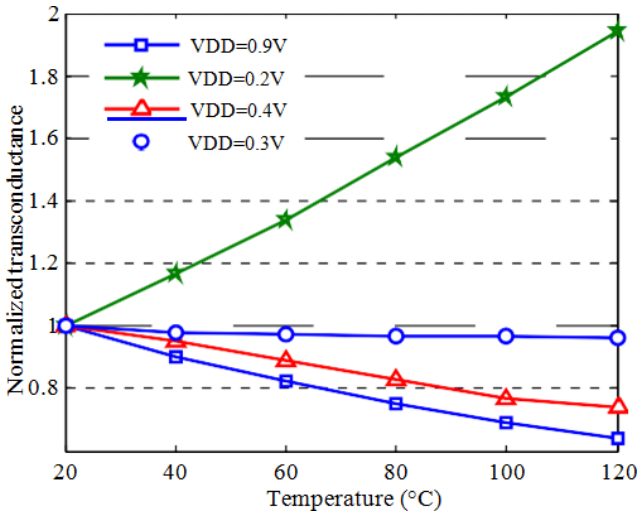


Fig. 6 Transconductance as a function of temperature

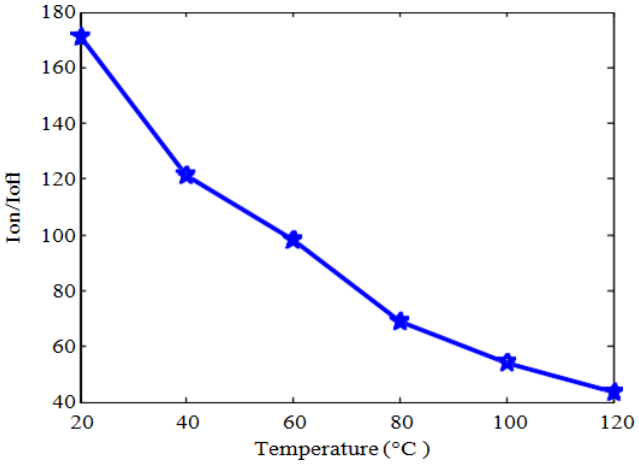


Fig. 7 ION/IOFF as a function of temperature at VDD=0.2V

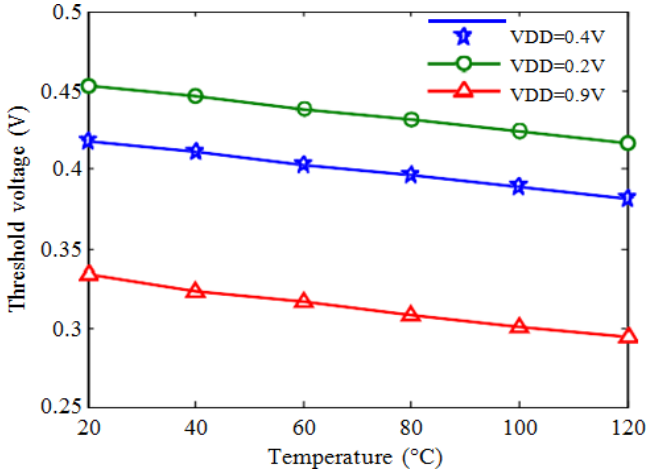


Fig. 8 Threshold voltage as a function of temperature

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Fig. 9 and 10 show the effect of temperature variation on the delay and power dissipation of an inverter. It is clear from Fig.9 that in deep sub threshold region (VDD = 0.1V), delaydecreases by 66.9%. However, in moderate subthreshold(VDD=0.4V) region, increasing temperature from 20°C to 120°C, the delay only increases by 13% due to decrease in drive current as shown in Fig. 7. Hence, to minimize the effect of temperature variation, it is necessary to operate a circuit in moderate subthreshold region instead of deep subthreshold and near to subthreshold region. As shown in Fig. 10, it can be observed that as temperature increases, power dissipation increases significantly. It has been also observed that at VDD = 0.1V, percentage increase in power dissipation is higher over VD = 0.4V. Hence, power delay product significantly rises at lower VDD as shown in Fig. 11. Fig. 12 shows the effect of temperature variation on Voltage Transfer Characteristics (VTC) of an inverter. It has been observed that switching threshold of inverter is not very much affected by the increase in temperature. However, it has also been observed from Fig.12 that noise margin decreases with the increase in temperature. Fig. 13 shows the effect of temperature variation

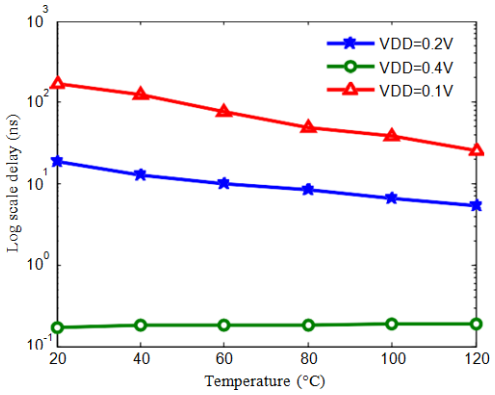


Fig. 9 Effect of temperature variation on inverter delay

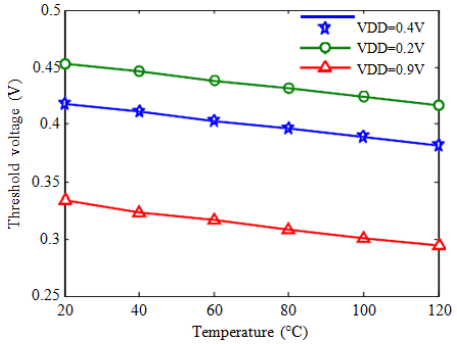


Fig. 10 Effect of temperature on power dissipation of an inverter

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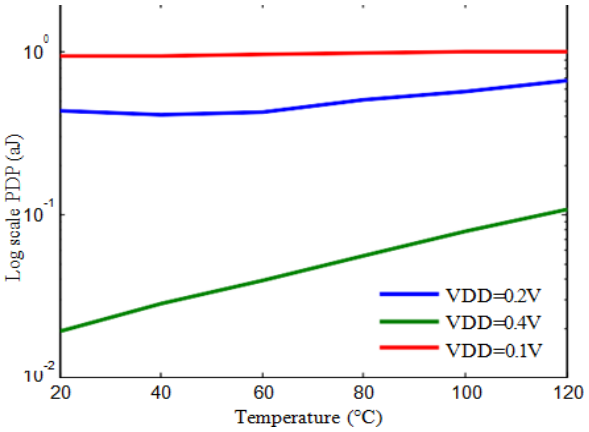


Fig. 11 Effect of temperature on PDP of an inverter

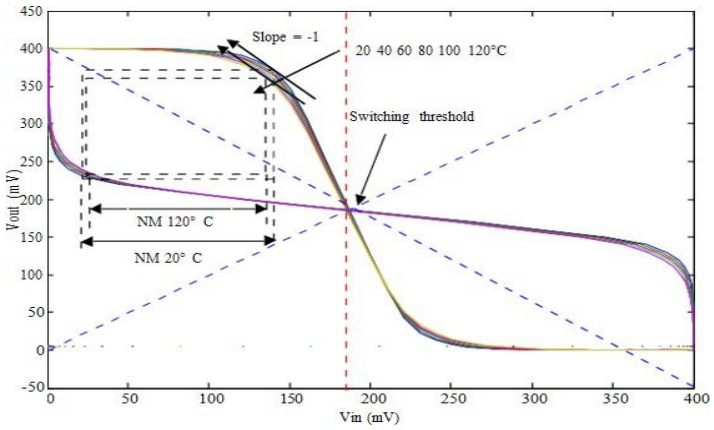


Fig. 12 Effect of temperature on noise margin of an inverter

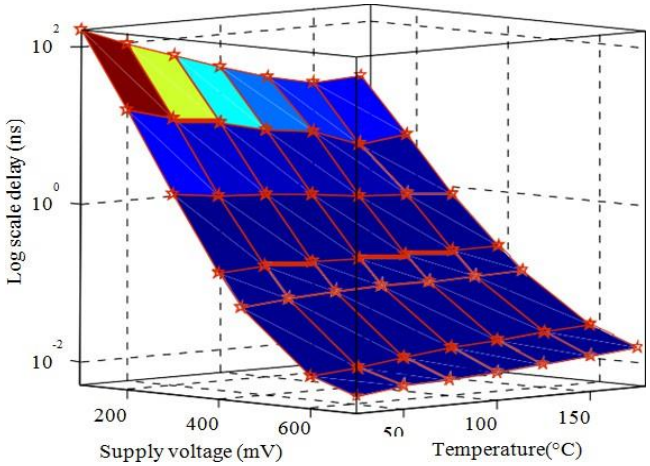


Fig. 13 Effect of temperature on delay at different voltages

On delay across the third inverter in the chain of five inverters. It is clear that the delay variation is less in moderate subthreshold regime compared to deep subthreshold and near threshold voltage regions.

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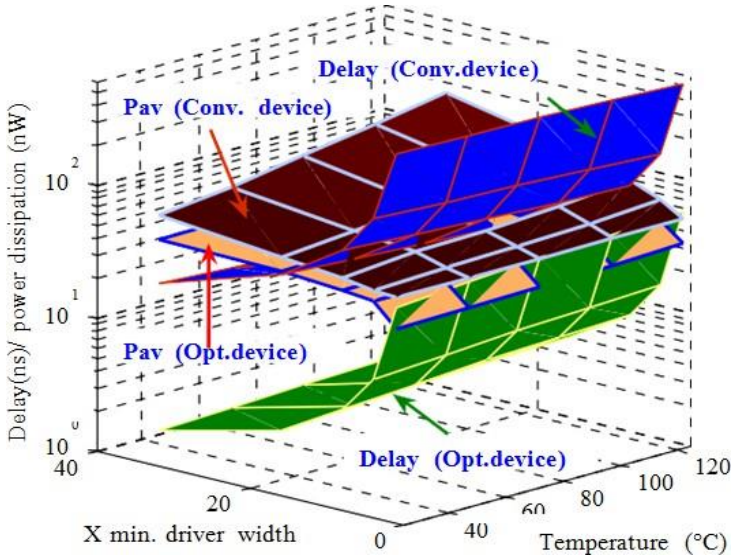


Fig. 14 Effect of temperature on delay and power dissipation at different driver width

The need to optimise the device for minimal temperature effects is evident from the previous section. Additionally, we have already investigated the performance of the interconnect driver at various temperatures and optimised the device's oxide thickness and threshold voltage in previous work [11]. Figure 14 [14] depicts the delay and power variability at various temperatures. It has been demonstrated that moderate, subthreshold, region-based driver operation significantly lessens the impact of temperature variation.

CONCLUSION

The impact of temperature changes on subthreshold device and circuit performance at various supply voltages has been effectively investigated in this work.

The performance of subthreshold circuits in the deep subthreshold area and close to the threshold voltage regions has been reported to be considerably impacted by temperature change. Si-NMOS device I-V characteristics demonstrate that running a subthreshold device in a moderate subthreshold zone considerably lowers the influence of temperature fluctuation. Based on the gate overdrive voltage, the subthreshold region exhibits both positive and negative temperature dependence. Therefore, an ideal supply voltage is required to design in the moderate subthreshold range in order to limit the impacts of temperature change on subthreshold circuit performance. Temperature rise minimises the noise margin brought on by high device OFF current. Additionally, it has been shown

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that changes in temperature have no impact on an inverter's switching threshold voltage.

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