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Heterogeneous Fir Digital Filter Simulation and Design in VHDL for DSP Applications

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Abstract

A basic building component of digital circuits such as ALU, microprocessors and microcontrollers, DSP processors, and various arithmetic operations is an added. The essential component of the arithmetic circuits is the full adder. The simplest cell of arithmetic circuits is the whole adder circuit. Many applications require logic circuits with a tiny chip size, fast throughput, and low power usage. The study focuses on the development of a 16-bit ripple carry adder based on the homogeneous adder idea. The chip is designed in Xilinx ISE 14.2 using VHDL and simulated in Modelsim 10.1. To validate the results, the design is generated on SPARTAN - 3E FPGA.

Keywords: *Digital Signal Processing, Ripple Carry Adder, FPGA, VHDL programming*

INTRODUCTION

Adders are the fundamental building blocks of digital applications and microprocessor computers. These systems make use of half adders and complete adders. Half adders and full adders [1, 2] are combinational circuits that provide the sum and carry of two and three bit binary sums, respectively. The parallel adder or the ripple carries adder is used to add the bigger bit data. The adder is utilised in a variety of DSP applications, including filter design [3].

The ripple carry adder's basic component is the full adder. Full adder [4, 5] is a combinational logic device that accepts three binary bits and outputs sum and

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carry. Figure 1 depicts the logic diagram, and Table 1 depicts the behaviour of the entire adder. The logical expressions are provided using equations (1) and (2). (2).

Table 1 Truth table of full adder

Input			Output	
a	**B**	**C**	**sum**	**carry**
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

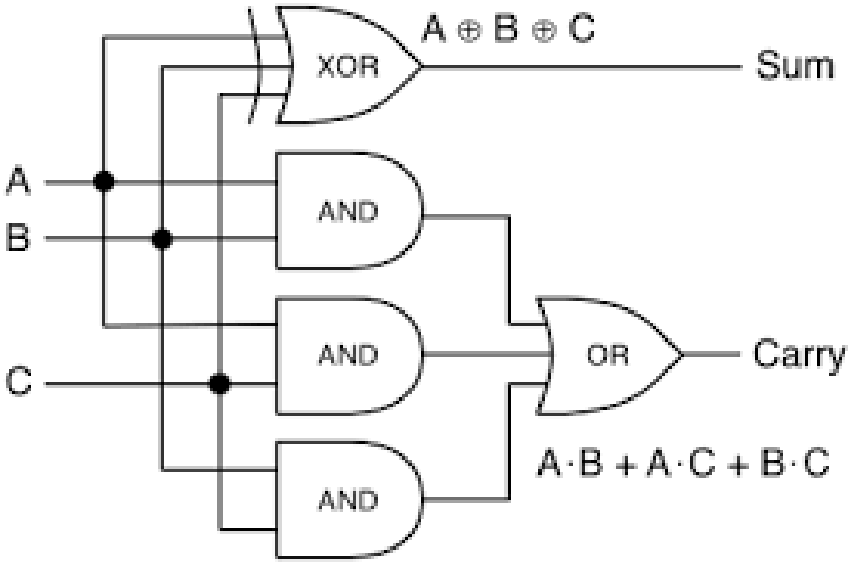


Fig. 1 Logic diagram of full adder

$$sum = \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc = a \oplus b \oplus c \quad (1)$$

$$car = \bar{a}bc + a\bar{b}c + abc\bar{} + abc = ab + bc + ca \quad (2)$$

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RIPPLE CARRY ADDER (RCA)

The design of the FIR filter [8, 10] is carried out using Ripple Carry Adder (RCA) instead of the decimal adder. The RCA will accept the 4-bit data as shown in Fig. 3 The 4-bit adder using full adder circuits can add two 4-bit numbers resulting in a 4- bit sum and a carry. Hence the sum by each full adder is performed simultaneously. This circuit is called the parallel adder or ripple carry adder. In a 4-bit parallel binary adder circuit, the input of each full adder will be Ai, Bi, and Ci, and the outputs will be Si and Ci+1, where i vary from 0 to 3. The carry of the previous stage is associated with a carry input of the succeeding stage. In the first stage A0, B0 and C0 (or C0 = Cin, which is 0) are added resulting sum S0 and carry C1. This carry C1 becomes the carry input to the second stage. In the same way, the second stage A1, B1 and C1 are added resulting S1 and C2. Carry C2 is the input for the third stage. A2, B2, and C2 are added resulting S2 and C3. Carry C3 is carried in the fourth stage. A3, B3, and C3 are added and resulting in S3 and C4. Here, C4 acts as a carry-out or Cout. Thus, this circuit results in a sum (S3S2S1S0) and a carry Cout.

REALIZATION OF 16-BIT HOMOGENOUS ADDER

In the same way, 16-bit ripple adder can be designed using either direct 16 number of full adders based on the concept of 4-bit RCA or it is also possible to use the cascade structure shown in the Fig. 4. In which 4 RCA are used in which RCA1 performs the addition of x(3:0) and y(3:0), RCA2 adds x(7:4) and y(7:4), RCA3 adds x(11:8) and y (11:8) and RCA4 performs x(15:12) and y (15:12). The output of the RCA1, RCA2, RCA3 and RCA4 give the out of sum Sout (3:0), Sout (7:4), Sout (11:8), and Sout (15:12). The output carry of one RCA is given as the input to the next RCA. In the RCA as the length In creases, there are the chances that the delay will increase. The delay calculation for the 'N' bit RCA is given by the Eq. (3)

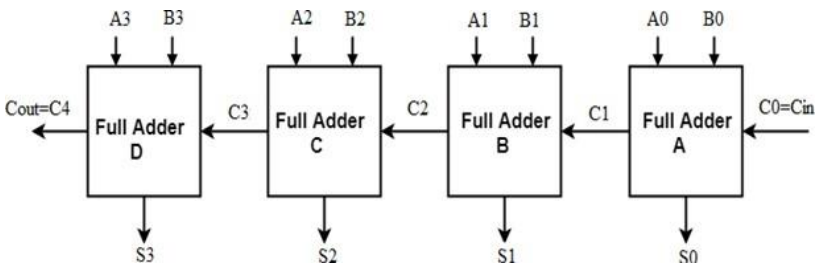


Fig. 2 Four-bit binary adder or Parallel binary adder

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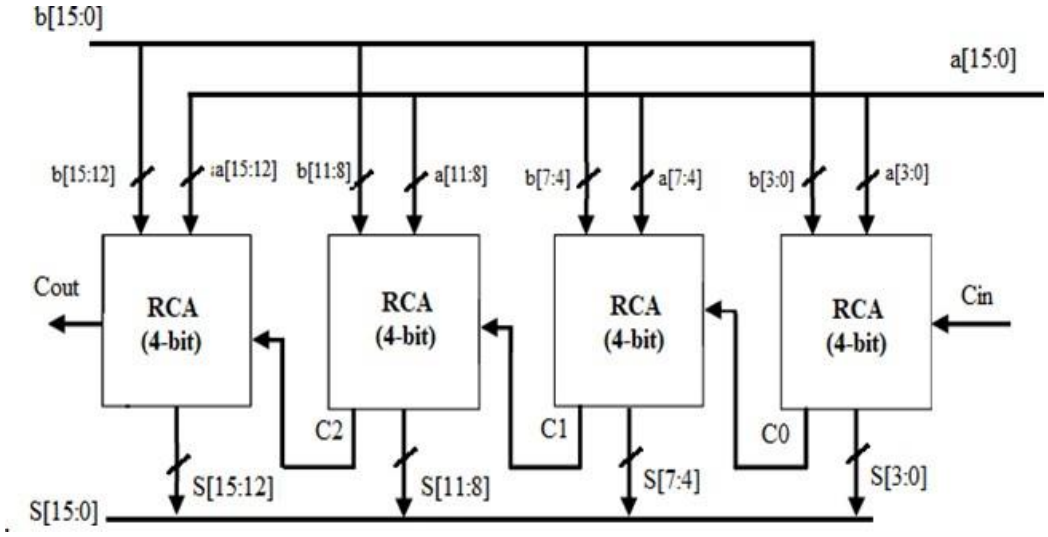


Fig. 3 Homogenous adder-based structure (16 bit)

$T_{logic} = T_{Fulladder}((x_0, y_0)\ to\ c_0) + (n-2) \times T_{Fulladder}(C_{in}\ to\ C_{out}) + T_{Fulladder}(C_{in}\ to\ S_{ou}(n-1))$ (4.3)

In this equation, $TFullAdder$ presents the delay of the full adder for the specified input and output with respect to the path of I/O.

RESULTS & DISCUSSIONS

The Xilinx software provides the RTL of the developed chip of adder which is depicted in the fig. 4 and internals schematic is also presented in the fig.5. The RTL provides the complete information of the input and output pins used in the design. The description of all the pins is given in table 2. The waveform simulation of the same is given in fig.6

The Xilinx software gives the details of the hardware utilization for the homogenous adder based 16-bit ripple carry adder. The table 3 provides the details of hardware summary and timing values. The hardware parameter slices, LUTs, memory and bounded input/output (IoBs), and 1-bit XOR2. Fig.7 presents the graph for the hardware resources. The combinational time presents the logic delay and routing delay from input to output. The information is directly extracted from the software with the target device on SPARTAN 3E FPGA.

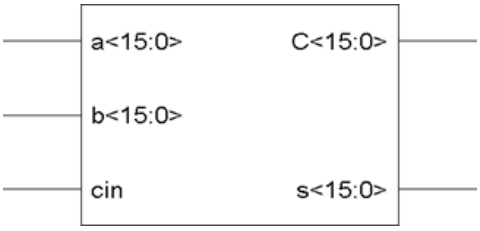


Fig.4 RTL view of adder

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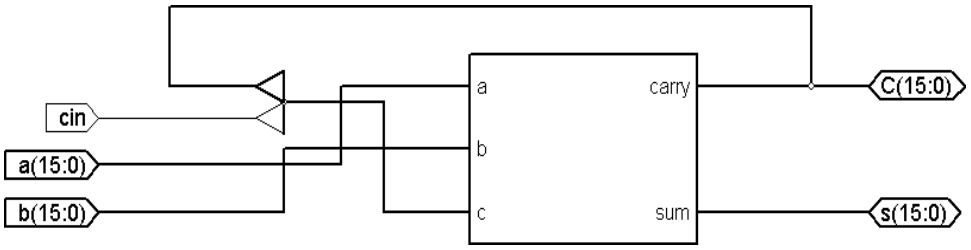


Fig.5 Internal schematic of 16-bit adder

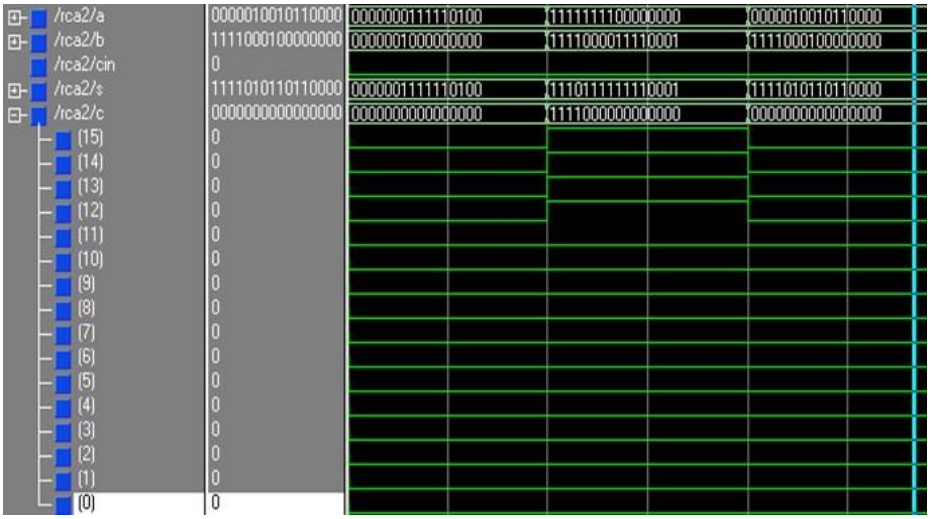


Fig.6 Modelsim waveform simulation of 16-bit adder

Test input-1: a = 0000000111110100 and b = 0000001000000000 then output s = 0000001111110100 Test input-2: a = 1111111100000000 and b = 1111000011110001 then output s = 1111000000000000 Test input-3: a = 0000010010110000 and b = 1111000100000000 then output s = 1111010110110000

Table 2 Pin details of the chip

Pin	Description
A[15:0]	It is the first 16-bit input of the adder. It is of the std_logic_vector data type.
B[15:0]	It is the second 16-bit input of the adder. It is of the std_logic_vector data
type. Cin	It is the input carry, considered as Cin = 0. It is of std_logic.
S[15:0]	It is the adder output of 16-bit. It is of the std_logic_vector data type.
C[15:0]	It is 16-bit outputs considered as an intermediate carry of the adder including output carry as C[15]. It is of the std_logic_vector data type.

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Table 3 Xilinx software parameters for 16- bit adder

Parameter	16-bit Homogenous Adder
Slices Usage	23
LUTs Usage	40
IoBs	65
1 bit XOR2	16
Memory Usage	111572 kB
Combinational time	36.323 ns

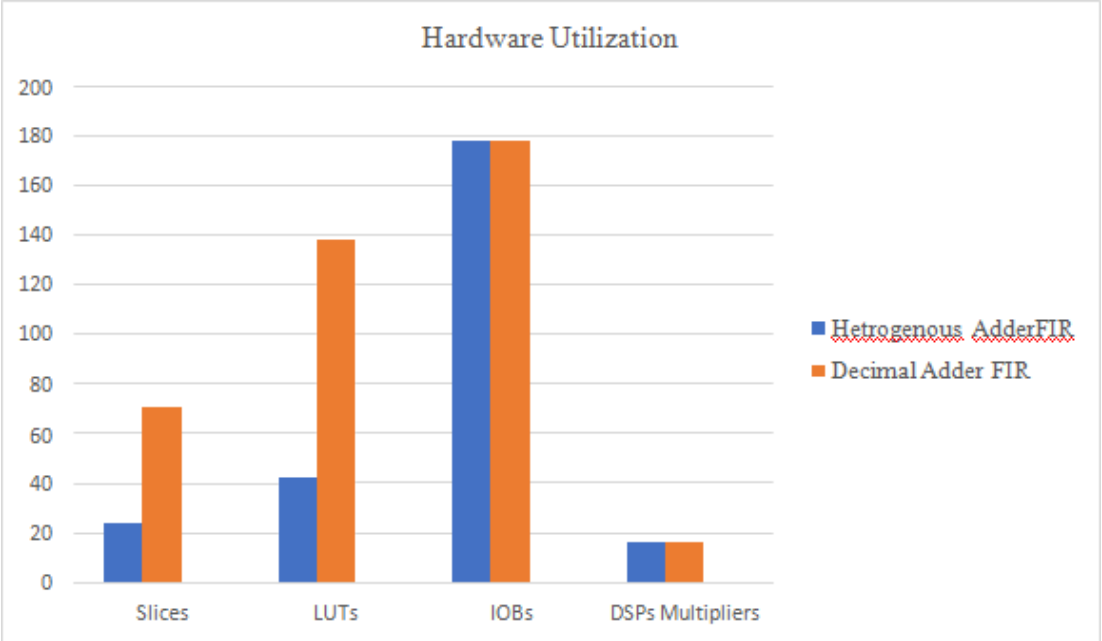


Fig.7 Hardware usage curve with different parameters

CONCLUSIONS

The design of a 16-bit homogeneous ripple carry adder was successfully completed in Xilinx ISE 14.2. The output of the adder is simulated in modelsim10.1 programme for various scenarios. The design employs a cascading technique of the same sort of full adder circuits to construct the 4 bit ripple carry adder, which is then used to implement the 16 bit adder. This design may be used in a variety of digital circuit and DSP-based communication systems. The intended chip was successfully generated on SPARTAN-3E FPGA, with device parameters such as slices, device LUT, IoBs, and XOR gate being 23, 40, 65, and 16 correspondingly. The design makes use of 111572 kB of memory, and

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the combinational route time is 36.323 ns. The created device will be useful for signal processing applications that need addition as a building block and calculations, such as FIR filter design, DFT method, and FFT computations that involve large scale adders and multipliers.

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