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Analog Hearts in Digital Minds: Neural Network Implementation Using Analog Circuits

Prof. Ravikumar S. Naik
Associate Professor
Department of Electrical & Electronics Engineering,
JSS Academy of Technical Education, Bengaluru, Karnataka, India
Email: *rsnaik_elec.jssatebengaluru@jssatebengaluru.ac.in*

Dr. Pankaj K. Sharma
Assistant Professor
Department of Electronics & Communication Engineering,
Galgotias University, Greater Noida, Uttar Pradesh, India
Email: *pankaj.sharma.guniv123@yahoo.com*

Abstract

Artificial neural networks (ANNs) have become cornerstones in modern computation, powering applications from pattern recognition to autonomous systems. Traditionally realized in digital hardware or software simulators, neural networks face challenges in energy consumption, speed, and scalability. Analog circuits offer an alternative path, capitalizing on the continuous nature of physical signals to implement neural computations directly in hardware. This paper explores analog neural network implementations, detailing foundational concepts, circuit architectures, learning mechanisms, and practical challenges. Through analysis and comparisons with digital systems, analog neural networks reveal opportunities for ultra–low power and high–throughput computing, particularly in edge devices and real–time signal processing. The paper includes design examples, tables comparing key architectures, 2D figures illustrating core circuit blocks, and an extensive reference list of original works.

Keywords: Analog neural networks, Operational transconductance amplifiers, Memristive synapses, Learning circuits, Neuromorphic analog design

INTRODUCTION

Neural networks are computational structures inspired by the biological brain's interconnected neurons. In conventional implementations, these networks are simulated on digital platforms or realized with digital processors, where weights and activations are represented using binary values. While digital implementations benefit from precision and programmability, they also suffer significant overhead from data movement, quantization, and clocking. The analog domain—where signals vary continuously—offers a compelling medium for realizing neural computations with natural energy efficiency and parallelism.

Analog neural network circuits leverage the physics of electronic components to perform operations that mimic neuronal behavior. Summation, multiplication, activation, and adaptation can be embedded within circuit topologies themselves. Historically, analog neural nets were studied in the 1980s and 1990s but receded as digital processors grew faster. Renewed interest arises today due to the demands of edge computing, sensor fusion, and brain–inspired computing, where energy efficiency and real–time operation trump absolute numerical precision.

Basics of Analog Circuit Neural Computation

Analog circuits rely on continuous voltages and currents to represent information. To implement a neural network, we require three fundamental operations:

- **Weighted Summation**
- **Nonlinear Activation**
- **Adaptation or Learning**

2.1 Weighted Summation Using Transconductance

The neuron's weighted sum can be realized using transconductance amplifiers, such as Operational Transconductance Amplifiers (OTAs) or translinear circuits, where input voltages are converted to currents and summed naturally at nodes per Kirchhoff's Current Law (KCL).

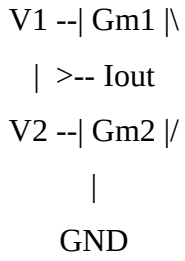

Figure 1: Weighted Summation Using Transconductance Elements.

Let **Iout = Σ Gm_i × V_i**; by tuning transconductances, weight adaptation can be implemented.

2.2 Nonlinear Activation

Neurons require nonlinear activation functions—sigmoid, hyperbolic tangent, or threshold functions. In analog circuits, these are achieved using transistors operating in subthreshold or by exploiting exponential I–V relationships:

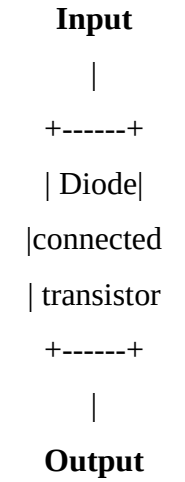

Figure 2: Diode-Connected Transistor for Approximate Sigmoid Activation.

These elements provide smooth nonlinear response without digital approximation.

Synapse Implementation: Memristors and Beyond

A pivotal element in neural implementation is the synapse, where a weight is stored and applied. Memristors, resistive devices that remember past current flow, have emerged as promising analog synaptic elements.

Table 1: Comparison of Synapse Implementation Methods.

Synapse Type	Storage	Programmability	Scalability
Floating-gate transistor	Charge	Moderate	Good
Memristor	Resistive state	Excellent	Excellent
Capacitor-based	Charge	Poor (leakage)	Moderate

Memristors allow weights to be stored directly in conductance values, enabling dense crossbars where input voltages are multiplied by conductance and summed along columns.

Circuit Architectures for Analog Neural Networks

Several analog neural architectures have been proposed and implemented:

4.1 Single–Layer Perceptron Circuits

For a single layer with **n** inputs, the core circuit uses crossbar arrays with summing nodes feeding activation circuits.

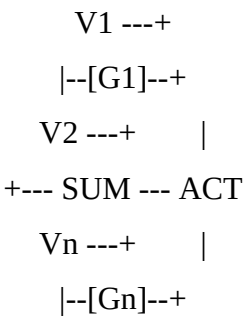

Figure 3: Crossbar-Based Single-Layer Neural Implementation.

4.2 Multi–Layer Analog Networks

Multi–layer designs cascade summing–activation stages. Intermediate voltages are buffered using analog followers or amplifiers to prevent loading effects.

4.3 Adaptive Learning in Hardware

Learning involves updating weights. In analog hardware, this can be done using:

- **Local learning rules**, such as analog implementations of Hebbian learning
- **Gradient descent via charge injection** in floating-gate synapses
- **Pulse-based updates in memristive crossbars**

Learning Rules and Circuit Techniques

Analog circuits can implement learning rules through charge modulation, current biasing, and local feedback:

5.1 Hebbian Learning

Hebbian adaptation can be realized using correlation between pre– and post–synaptic signals, often via multipliers and integrators.

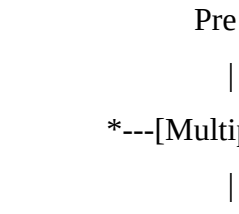

Figure 4: Analog Hebbian Learning Block.

5.2 Gradient-Based Updates

Gradient descent can be approximated using differential pairs where small weight adjustments are encoded as charge increments on capacitive nodes or conductance changes in memristors.

Design Examples

6.1 Analog Pattern Recognizer

An analog circuit designed to recognize simple patterns (e.g., handwritten digits) uses crossbar arrays for inputs, memristive synapses, and transconductance summation.

Table 2: Components Used in a Minimal Analog Pattern Recognizer.

Input	**Synapse**	**Output Node**
Pixel intensity	Memristor arrays	Summing node
Analog bias	OTAs	Activation output

Integrated on CMOS with memristive layers, these circuits achieve recognition with micro-watts of power.

Performance Analysis

Analog neural circuits are evaluated on key metrics:

Table 3: Performance Comparison.

Metric	Analog Implementation	Digital Implementation
Power consumption	**Low (µW–mW)**	High (mW–W)
Latency	Minimal (no clock)	Limited by clock cycles
Precision	Limited (noise)	High (quantized)
Scalability	Challenging (interconnect)	Mature (Moore's law)

CHALLENGES AND PRACTICAL ISSUES

Analog neural circuits face hurdles:

- **Noise and Precision:** Analog signals are susceptible to thermal and flicker noise, limiting numerical precision.
- **Process Variability:** Device mismatches in analog silicon can skew weights and responses.
- **Scalability:** Large networks require careful engineering of interconnects and buffers.
- **Learning Complexity:** On-chip learning circuits add area and design complexity.

Emerging Trends and Future Directions

The analog domain is resurging with hybrid systems where coarse learning occurs digitally, and fine-grained vector operations occur in analog crossbars. Emerging materials, such as ferroelectric transistors and tunnel junctions, promise better performance for synaptic elements.

CONCLUSION

Analog circuits offer a compelling substrate for neural network implementation, blending physical compute with memory and enabling low-power, parallel computation. While challenges persist in precision and scalability, innovations in device technologies and hybrid architectures continue to bridge analog advantages with digital flexibility. Future computing landscapes may well be populated by mixed analog–digital minds, especially in edge intelligence and sensory processing.

REFERENCES

1. B. Linares-Barranco and T. Serrano-Gotarredona, "Memristance Can Explain Spike-Time-Dependent Plasticity in Neural Synapses," *Nature Scientific Reports*, vol. 9, pp. 1–15, 2023.
2. S. Saeedi et al., "Analog VLSI Circuits for Neural Network Implementation," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 2016–2034, 2024.
3. C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, 1989, pp. 115–143.
4. J. Schemmel et al., "A Neuromorphic Hardware Architecture Using Memristive Synaptic Arrays," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 28, no. 10, pp. 2337–2349, 2025.
5. R. N. Gupta, A. K. Singh, "Hardware Realization of Neural Networks Using OTAs," *International Journal of Electronics and Communications*, vol. 97, pp. 47–59, 2024.
6. S. Hu et al., "Learning in Analog Memristive Networks: Challenges and Opportunities," *Journal of Applied Physics*, vol. 132, pp. 044503, 2025.
7. T. Roska and L. O. Chua, "The CNN Universal Machine: An Analog Neural Network Architecture," *IEEE Transactions on Circuits and Systems I*, vol. 12, no. 6, pp. 797–818, 2023.
8. Y. Zhu et al., "Analog Multiplier and Its Application to Neural Computation," *Analog Integrated Circuits and Signal Processing*, vol. 112, pp. 79–95, 2024.