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The Interconnect Data Network Architecture for Parallel Systems

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Abstract

The performances of various multiprocessor architectures by taking into account their topological properties. It is evaluated that, an interconnect data network is giving better performance in terms of nodes and average distance. Whereas, better performance in terms of diameter and message traffic and density respectively. The option of the interconnect data network may affect as node complexity, bisection width, scalability, switching model, degree, cost of network etc. And, they design high performance interconnection network, which can be used in designing of multiprocessor server.

Keywords: *Interconnect Data Network, Parallel Systems, Subsystems, Processor*

INTRODUCTION

An interconnection network is exploiting for interchanging data between two processors in a multistage network. Memory bottleneck data network is a basic shortcoming of Von Newman architecture. In case of multiprocessor systems, the showing will be severely affected in case the data interchange between processors is delayed. The multiprocessor system has one universal shared memory and each and every processor has a small local memory. In this, paper the processor can bout the data from associated memory with another processor or from shared memory using an interconnection network. Thus, interconnection networks play a essential role in resolute the overall performance of the multiprocessor systems. The interconnection networks are useful network systems containing of nodes and edges. The nodes are switches in network having few input and few output say ‘n’ input and ‘m’ output lines. Data is depending on processor and switch connection for data forwarding from input lines to output lines. The interconnection network is placed between different devices in the multiprocessor network.

The network is created with links and switches, which helps to send the information and data from the source node to the destination node. Here we specified networks by its topology, routing algorithm, switching strategy, and flow control mechanism. Interconnection networks are formulated by three basic components:

- A link is a cable of one or multi optical fibers or electrical wires with a connector at each end point attached to a switch or network interface port. Though this, an analogy signal is transmitted from one end and received at the other to obtain the original digital information.

- A switch is made up of a set of input and output ports, an internal “cross-bar” connected with all input and output, internal buffering, and control logic to effect the input/output connection at each port point in time.

- The network interface controls the packets and constructs the path and control information. It may have both input/output buffering and compared to a switch.

INTERCONNECT DATA NETWORK

In my opinion; the interconnect data networks refers to some nodes which using network equipments, such as, switches/routers and communication channels. However, I think their difference come from the types of their nodes. The nodes in data networks are servers; but, those in interconnection networks are processors and memory modules. In addition, some unique issues just are in data networks such as security, cooling system and so on.

According to the explanation of “Interconnect Data Network”, we are found across a wide scope of applications; which are broadly used to connect processors and recollections in multiprocessors as switching textures for line routers and switches for connecting gadgets and for on-chip networks. The result of their various applications, the inherent supposed madness of advanced communication systems, leads to a conclusion, not a cause or memories; the next Generation Processor Memory [4].

According to the Moore's Law; "The number of accessible semiconductors growing exponentially over the long haul". For this reason, nets with a simpler scale Interconnect gently than, the diameter of the rope to follow regularly time. So, the interconnection networks has become an important factor for determining and vulnerable overall cost of the system in a Multiprocessor computer system, as processor and memory execution continues to increase, the presentation of the interconnection network assumes a focal part in determining the general exhibition, just as the expense of the system.

Apart from this, we also say; the network and bandwidth inheritance often causes RAM and bandwidth to be disabled, this also works for chip networks. As the number of components integrated into a chip increases, the chip network connecting these components will form the basis for determining the future exposure value of multicenter processors. Running beyond 1/3 of the total connection costs can be a huge cost to systems. Thus, it is vital to reduce the costs of the overall system cost chains.

In addition, as the number of surround nodes of the surrounding will increase, future regional and high-performance multiprocessor processors should be considered. Pay attention to what innovation means for interconnected networks, and how innovation models can be leveraged to reduce the costs and unemployment of interconnected networks and create more efficient systems. In distributed-memory architecture, processing elements are linked together by an interconnection network. Now, in this research work we define the terminology that will be used during the discussion of interconnection networks.

INTERCONNECT DATA NETWORK TOPOLOGY

Apart from the above, we can also define; "An interconnect network topology is <Sn, En> in a finite set 'Sn' of destination nodes together with an adjacency relation. Those nodes are stands in the surrounding of natural world that means whole of the countries which are connected from here to there and serves data with different communication links and medium. Where is {En ⊆Sn X Sn} on the set. If (a, b) are nodes such that (a, b) ε y, then, we say that, there is a direct edge from a to b2. Infrequently, all edges in a particular topology will be undirected, meaning that both (a, b) ε y and (b,a) ε y. Else, here we will treat all edges as undirected. If two nodes are connected by an edge, then, we called them Adjacent. Now, in short we were defining the properties; that determine their usefulness for particular applications.

- It is a way from different destination no to nx, it is a sequence of destinations no, n1…………., nx i.e., for (1 ⩽ k ⩽ x); in here (nx) is the adjacent node to (nx+1) and, edge is the length of the path not the number of nodes.
- It is the maximum number of edges that are incident to a destination node with various applied topology.
- It is the length between the shortest point-to-point entire destinations.
- It is the largest distance between any two destination nodes in that networks which is applied.
- It is the smallest number of edges that must be deleted to dissociate the set of nodes into two equal size sets, or size during by at most one node.

On my thinking and my research; we can say all data must pass sequentially through the bottle edge neck, like a one-lane bridge in the middle of a four-lane highway. In contrast if the bisection width is high, then many edges must be removed to split the destination node set. That means; there are many paths from one side of the set to the other side and data can go in a high degree of parallelism from any one half of the nodes to the other.

But, apart from this we also see a network topology is the game plans of the different communication media either medium of a static or dynamic network. Basically, it is the topological design of network architecture, and might be portrayed physically or logically. Where, static network alludes to the situation of different network components, including gadget location and link installation, while the dynamic network shows how information streams within a network, paying little heed to its physical plan. Distances between hubs, physical interconnections, transmission rates, and/or signal sorts may contrast between two networks, yet their geographies might be indistinguishable.

According to my view; a genuine model is a neighborhood but some random hub has at least one physical links to other gadgets in the network; graphically mapping these links brings about a mathematical shape that can be utilized to describe the physical topology of the network. Conversely, mapping of the information stream between the components determines the logical topological network. There are two essential classifications of network geographies i.e.

- It is the state of the cabling design used to link gadgets and it also alludes to the design of cabling, the locations of hubs, and the interconnections between the hubs and the cabling.

- It is the way that signs follow up on the network media, or the way that the information goes through the network starting with one gadget then onto the next regardless interconnection of the gadgets.

A. It is a way to selecting best ways in an applied or assigned network in the surrounds. According to my way of explanations; it was additionally used to mean forwarding network traffic. However; this last feature has been significantly improved and is described as “Transfer of Data’s”. Routing is performed for different assigned networks, including circuit switching, electronic information networks, and transportation networks. It is concerned fundamentally with routing in electronic information networks using parcel switching innovation. In a bundle switching networks, routing coordinates parcel forwarding through intermediate and fastest hubs. The routing interaction generally coordinates on routing tables, which maintain an address of destinations nodes. Along these lines, constructing routing tables, which are held in the switch's memory, is vital for proficient routing.

B. It is an efficient and fast technique in most of fundamental necessity to accomplish great execution from an interconnection network. In this system that moves information from an input channel and to yield channel. Network latencies are profoundly subject to switching technique. Otherwise i.e., wormhole routing has become the dominant switching technique utilized in contemporary multi destination nodes. This is because it has low buffering necessities, and all the more critically, here dormancy becomes independent of the message distance.

C. It is a synchronization protocol for transmitting and receiving a unit of information. The unit of flow control alludes, to that portion of the message whose move should be synchronized. The channels and buffers are the distinct advantages of an interconnection network where channels are utilized to transmit packets between nodes and buffers are executed within the nodes as capacity gadgets like registers or recollections. These capacity gadgets hold the packets incidentally at the nodes. An ideal flow control system should dodge the asset conflicts which may lead the channel to sit state and along these lines the general presentation of the topology may get influenced.

D. It is enables framework to continue intended operation, perhaps at a diminished level, rather than failing totally, when some piece of the framework fizzles. The term much completely operational with, maybe, a reduction in throughput or an increase in response time in case of some incomplete disappointment. That is, the framework in general isn't halted due to issues either in the hardware or the software.

Apart from the above expiations; at last we conclude as; wormhole routing depends on blocking instrument for flow control, it might bring about deadlock due to the cyclic conditions over network assets during message routing. A decent flow control procedure should meet some significant models like congestion reduction, reasonableness and deadlock evasion. The main reason for Virtual channels, in wormhole directed network, where to tackle the issue of deadlock. Flow control concerns techniques for dealing with contention among multiple directives for similar channels and buffers. Flow control techniques are profoundly subject to the switching plan utilized; in wormhole routing, the most common flow control procedure is the utilization of virtual channels.

According to the Parallel System definition; generally we have stringent dependability necessities as enormous investments are done in such systems. It additionally relies upon the idea of applications for which they are probably going to be utilized. Fault tolerant networks are fundamental for the dependability of parallel computer systems. Interconnection networks are all the more often composed of thousands of components-nodes, channels, routers, and connectors that all in all have disappointment rates higher than is satisfactory for the application. High accessibility or dependability is normally accomplished by some type of fault resilience, which helps the framework in managing the deficiency of at least one component without disruption in its operation. The accessibility, unwavering quality, and the presentation of the general framework rely upon the particular fault-resistance strategies utilized in the framework. A fault tolerant network can course information regardless of whether certain network components come up short.

At last we say, the disappointment of a network component can bring about breakdown of the whole framework, if satisfactory measures are not given to handle to such disappointments. Fault can happen in a parallel computer framework in the PE, memory, I/O framework, or switch and channels of the interconnection network, and to be successful a fault tolerant plan should address every one of these subsystems. The techniques utilized for network fault resilience are either software based or hardware based. In software-based technique; a versatile routing algorithm is utilized, which utilizes multiple ways for a given pair of source and destination to evade faulty components. In hardware-based technique; the network is upgraded by additional hardware and gives sufficient excess in the original network to endure a certain number of faults.

INTERCONNECT DATA NETWORK CHARACTERISTICS

According to the definition of the word “Interconnect”; now we focus on actual and possible physical connections. An interconnection network is a system of links that connects one or more devices to each other for the purpose of inter-device communication. In the context of computer architecture, an interconnection network is used primarily to connect processors to processors, or to allow multiple processors to access one or more shared memory modules. Sometimes they are used to connect processors with locally attached memories to each other. The way that these entities are connected to each other has a significant on the cost, applicability, scalability, reliability, and performance of a parallel computer. In general, the entities that are connected to each other, whether they are processors or memories, will be called nodes. An interconnection network may be classified as shared or switched. A shared network can have at most one message on it at any time. For example, a bus is a shared network, as is traditional Ethernet. In contrast, a switched network allows point-to-point messages among pairs of nodes and therefore supports the transfer of multiple concurrent messages. Switched Ethernet is, as the name implies, a switched network. Shared networks are inferior to switched networks in terms of performance and scalability.

A. Topological Characteristics

According to the above explanation, we have some topological characteristics i.e;

- The maximum number of links originating from any node is known as degree of that node.

- The distance between a pair of nodes is the smallest number of links that must be traversed to get from one node to the other.

- The diameter of a network is the largest distance between two nodes. Low diameter is better, because the diameter puts a lower bound on the complexity of parallel algorithms requiring communication between arbitrary pairs of nodes.

- The bisection width of a network is the minimum number of edges that must be removed in order to divide the network into two halves. High bisection width is better, because in algorithms requiring large amounts of data movement, the size of the data set divided by the bisection width puts a lower bound on the complexity of the parallel algorithm.

B. Layout Characteristics

Apart from the above, while the topological characteristics provide useful information with respect to the routing algorithm about the underlying graph for a network. The layout characteristics provide insight into fabrication cost and scalability i.e.;

- The longest link between a pair of nodes, when the network is laid out in a plane is known as maximum wire length.

- Network area is the minimum area (or volume) consumed by the network when laid out in a plane.

- The link width is the width in bits of each link connecting a pair of nodes.

C. Dynamic Communication Performance:

The dynamic communication performance of an interconnection network depends on the routing concepts. Are as;

- The time required for a packet to send on the network is known as latency. Latency does not include the time packet waits in the injection and delivery buffers. Latency is measured in clock cycles.

- The rate of data transfer i.e., Throughput. It is the number of flits accepted by delivery buffers per cycle per node, at steady state. In general, latency and throughput are used to describe the performance of routing algorithms in an interconnection network.

ARCHITECTURE OF COMPLETE INTERCONNECT DATA NETWORKS

According to me; it is nothing but a network which connects every nodes and transfer data's from here to there. In such kinds of networks, every Hub is connected to any remaining nodes in the connected network. It conveys fast messages from source hub to any destination hub. The Complete Interconnection Networks are; costly as far as the number of links required for their construction. It ought to be that the number of connection links in is given by,

N (N-l)/2, i.e., 0(N)

Now, if we can consider a network, which consists of N nodes. Where every connected hub has degree (N-1), measurement is 1 and the bisection width is ff x fJ. See Figure: 1.1; the case of Complete Interconnection Data Networks for (N = 8). Here, now we explain the Figure: 1.1; they represent 8-nodes architecture for complete interconnect data network between the source node to destination nodes.

Where;

P0, P1, P2, P3, P4, P5, P6, and P7 are the interconnect data server nodes.

According to the Figure: 1.1; nodes are representing the source destination in natural surroundings. Those are interconnected with each other and serve data from here to there and also make a circuit. That's why we can say the interconnect data network is also a complete graph. In present scenario we use this kind of network in small to bigger level and perform batch of operation at a same time with multiple places. According to the Figure: 1., we have some results explain in a simple way i.e.,

- More Circuits have more and fast communication.
- More circuits have more complexity.
- More circuits have more robustness.
- More circuits have more expansive.

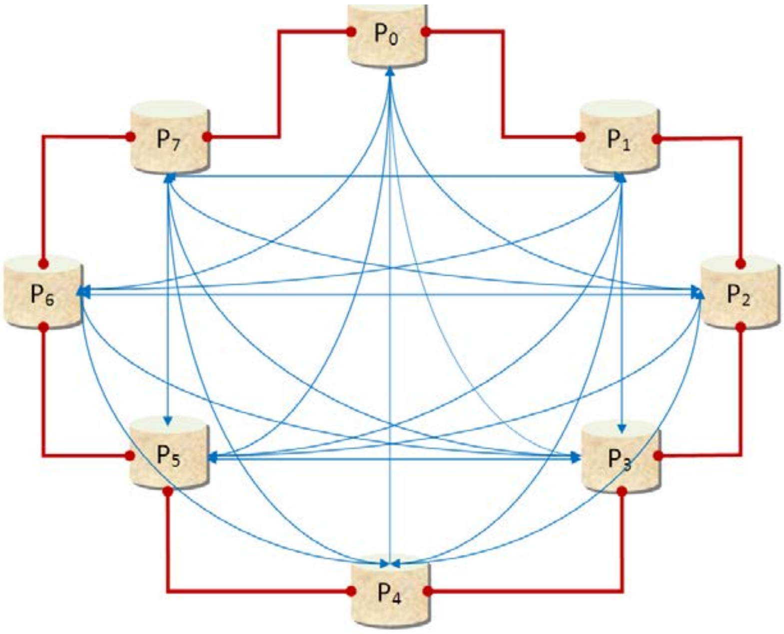

Figure: 1. Eight Nodes Architecture for Complete Interconnect Data Network

The above architecture construct in eight different destination nodes. It serves data to entire place in the surrounding in natural world as we says, their flow line define the medium of communication. The data destination nodes are similar to the country location of the all over the world which is connected via wired or wireless communication medium. According to my view, an interconnect data network is also an "Asynchronous System" that's why all different destination nodes machine can share their memory and clocks not in time. When it is synchronized then all machine should share in a time.

A. Binary (n-Cube) Data Network:

A binary n-cube data network is with 2n nodes arranged as the vertices of 'n' dimensional cube. In this an ordinary cube with the three-dimensional shape with control flow lines. Even though we probably think of cubes as a rectangular prism whose edges is all equal length i.e.; not the only way to think about it. Start from a single point can be a 0-cube; assume its label is 0. Now we assume; return this 0-cube, putting the copy at a distance away from one unit, and connecting both the original and the copy by a line segment of length 1, as shown in Figure: 2. We will give the duplicate node the label 1.

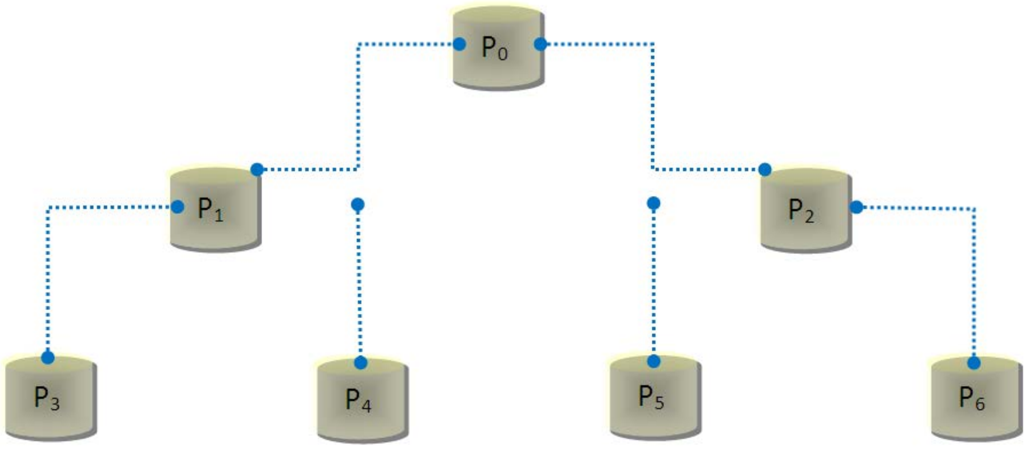

Figure: 2. Binary Architecture of Interconnect Data Network

Here, we have, replicate the 1-cube, putting the node parallel to the original at a distance away form1-unit in an orthogonal direction and connect corresponding nodes in the node to those in the original. We will use the binary numbers to label the nodes. The nodes in the cube will be denoted with the same labels as those of the original except for one change i.e., the most significant bit in the original will be changed from 0 to 1 in the cube, as shown in Figure: 2. Now, we repeat this procedure to create many more cubes or 3-cube i.e., here we replicate the 2-cube, putting the copy parallel to the original away from the distance of 1 unit, a way in the orthogonal direction. Then connect nodes in the corresponding nodes in the original, and start reliable all the nodes by adding one to another significant bit, 0 in the original and 1 in the cube.

It is now very simple to see how we can create hypercube by arbitrary dimension, although drawing them becomes a bit Herculaneum. Apart from this; the labelling of nodes will play an important role in for understood the binary cube. Observe some point;

- The labels of two nodes differ by exactly one bit change if and only if they are connected by an edge then the label of two nodes are differ by 1-bit.
- Node label is represented by n bits in any n dimensional binary cube. In which each node bits can be inverted (0>1 or 1>0), showing that each node has exactly ‘n’ incident edges.

- The diameter of an n-dimensional binary cube is ‘n’. Let observe that a given integer of node is represented with ‘n’ bits can be transformed to any

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other ‘n’-bit integer by changing at most ‘n’ bits, one bit at a time. This corresponds to a walk across n-edges in a binary cube from the first label to the second label.

- The bisection width of an n-dimensional binary cube is 2n−1. A way to see this is first realize that all nodes can be thought of as lying in one of two planes then pick any bit position and call it ‘x’. The nodes whose x-bit = 0 are in one plane, and those whose x-bit = 1 are in the other. To divide the network into two sets of nodes, one in each plane and one has to delete the edges connecting the two planes. Every node in the 0-plane of cube is attached to exactly one node in the 1-plane by one edge in the cube. Therefore we have 2n−1 such pairs of nodes, and hence 2n−1 edges. There is no smaller set of edges can be cut to split the node set.
- The number of edges in an n-dimensional binary cube is n *2n−1 .for this case we note that it is true when n = 0, when there are 0 edges in the 0-cube. Let Consider that, it is true for all k≤ n. A binary cube of dimension ‘n’ consists of two binary cubes of dimension n − 1 with one edge between each pair of nodes of corresponding nodes in the two smaller binary cubes. There are edges having2n−1. Thus, here we are using the inductive hypothesis, the binary cube of dimension ‘n’ has 2*(n−1)*2n−2+2n−1 = (n−1)*2n−1+2n−1 = (n−1+1) * 2n−1= n* 2 n−1 edges. so axiomatically of induction, it is proved.

One half the numbers of nodes of bisection width is very high, and the diameter is low. This makes the binary cube is an attractive organization. Wherever, the main drawback is that; the number of edges at per node is a logarithmic function of network size which making it difficult to scale up, and the maximum edge length increases as network is increases the size.

B. Butterfly Data Network:

It consists of (P + 1)2p nodes arranged in p + 1 ranks, each containing n = 2p nodes. Where, ‘p’ is the order of network. The ranks are labelled 0 through p according to the Figure: 3; depicts a butterfly network of order 4, meaning that it has 5 ranks with 24 = 16 nodes in each rank. The columns in the figure are labelled 0 through 15.

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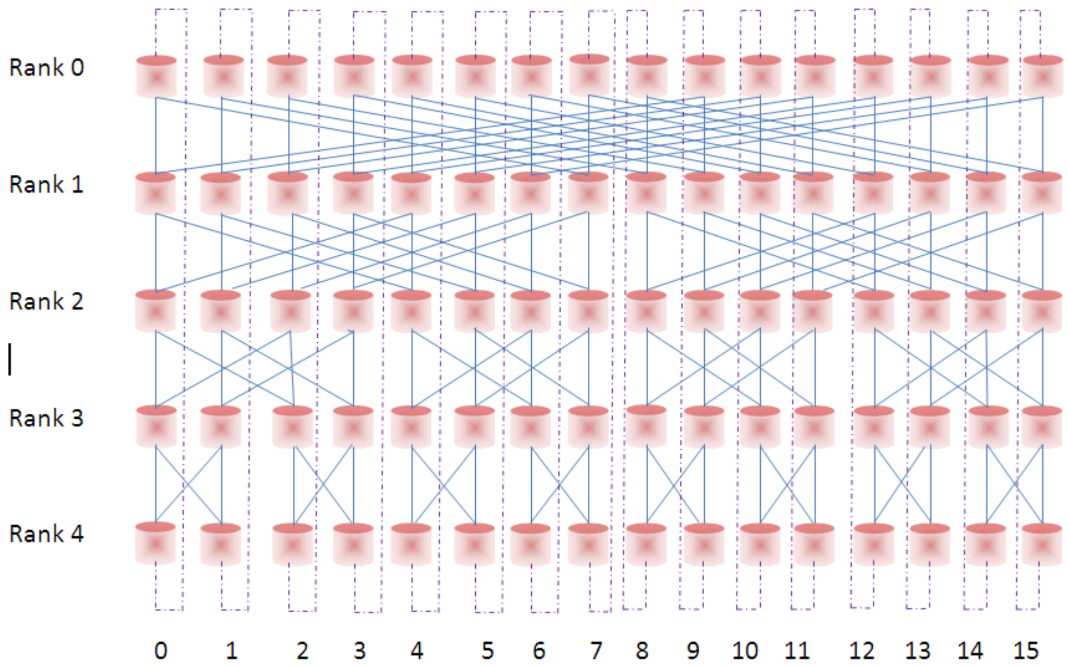

Figure: 3 Rank-4 Butterfly Data Network Architecture with Representing Same Node

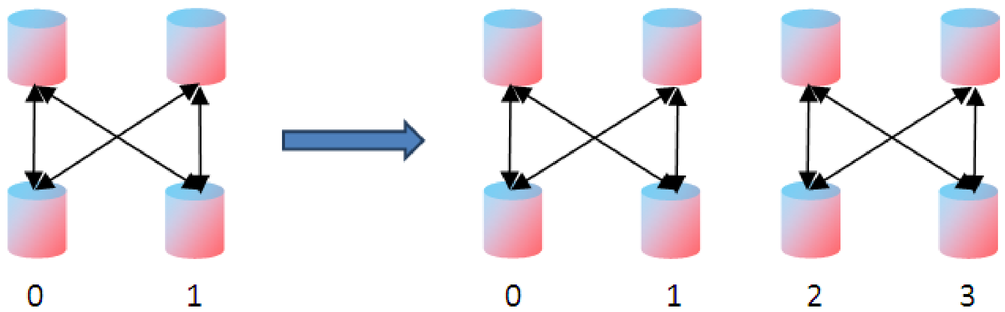

Figure: 4 Recursive Construction of Butterfly Data Network

Here, we describe two different methods for constructing a butterfly data network of order p.

Method-I:

- Create p + 1 ranks labelled 0 through p, each containing 2p nodes, which is labelled 0 through 2p − 1.
- Let, {r, s} denote the node in rank r, column s.
- For each rank, from 0 through p− 1, connect all nodes [r, s] to nodes [r + 1, s]. In other words, we can say draw the straight lines down the columns as shown in Figure: 3

- For each rank, from 0 through p− 1, connect each node [r, s] to node [r + 1, (s + 2p−r−1)]. This will creates the diagonal edges in graph matrix which form the butterfly pattern.

Method-II:

Here, we are defining recursive dentition of a buttery network

- In butterfly network with order 0 consists of a single node, labelled [0, 0].
- To form a butterfly network of order p + 1, replicate the butterfly network of order p, labelling the corresponding nodes in the copy by adding 2^p to their column numbers. Place the node to the right of the original, so that nodes remain in the same ranks. Add all rank numbers from 0 to n and create a new rank 0. For each S = 0, 1, , ..., 2^{p+1}, connect the node in column 'S' of the new rank 0 to two nodes: the node in rank 1, column 's' and the corresponding node in the copy.

It can be shown that there is a path from first to last node in the rank. If we take this case, then the diameter is 2p; to get from node 0 to node 15 in the first rank requires descending to rank 4 and returning along a different path. If, however, the last rank is really the same as the first rank, which is sometimes the case, then the diameter is p.

According to the Figure: 3; we are represents this type of network with dashed lines between the first to last ranks. The bisection width is 2p. To split the network requires deleting all edges that cross between columns $(2^{p-1} - 1)$ and (2^{p-1}). Only the nodes with rank 0 have connections that cross this divide. There are 2p nodes in rank 0, and one edge from which each node on the other side of the imaginary dividing line. This network topology has a fixed number of edges per node, 4 in total; nevertheless the maximum edge length will increase if the order of the network increases.

At last observing view in Figure: 3, now taking each column and enclosing it in a box. And, call each box is a node, where 2^p such nodes. So any edge that was incident to any node within the box is now considered incident to the new node to the box. The resulting network contains 2^p nodes connected in a p-dimensional binary cube. This is the relationship between butterfly and binary cube networks.

CONCLUSION

Apart from the above research, we have some results according to the above study interconnect data network in parallel system; whose processing units are transcript so that a single machine could consist of several thousand processing units all working on the same application in different destination. We have some results, are as;

- Processor arrays are suitable for only highly data parallel problems not those that have little data parallelism.
- When a program has a large fraction of conditionally-executed code then a processor array will not perform well.
- Processor arrays are designed to solve a single problem at a time in a batch style processing, because context switching is too costly on them.
- The cost of the both front end of a processor array and the interconnection network is high and this cost must be remuneration over many PEs to make it cost effective.
- One of the main reasons is that the control unit of a processor was costly to build because become popular. As control units have become less expensive, in compare to multiprocessor processor array price is down.

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