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Edge Computing Architectures for Ultra-Low-Latency Control in Automated Manufacturing Systems: A Comprehensive Review

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ABSTRACT

In the landscape of modern industrial automation, the proliferation of high-frequency data streams from cyber-physical systems has fundamentally stressed traditional centralized cloud computing architectures. For high-speed applications such as multi-axis motion synchronization, active vibration suppression, and real-time robotic trajectory corrections, relying on remote cloud networks introduces severe transmission jitter and non-deterministic propagation delays. This review paper provides a comprehensive, technically exhaustive analysis of Edge Computing Architectures specifically tailored to achieve ultra-low-latency control loops within automated manufacturing environments. We systematically examine the architectural configurations governing industrial edge deployments, contrasting embedded systems, localized edge gateways, and containerized fog computing layers. The paper evaluates key communication protocols, deterministic networking frameworks—including Time-Sensitive Networking (TSN) and EtherCAT—and hardware-software optimization pipelines designed to guarantee sub-millisecond execution deadlines. Furthermore, critical research gaps such as multi-node synchronization instability, edge-to-cloud security vulnerability, and hardware heterogeneity bottlenecks are identified. Finally, a robust structural roadmap is proposed to guide future research toward hyper-reliable, self-healing edge architectures capable of sustaining zero-defect production limits in the Industry 4.0 ecosystem.

KEYWORDS: *Edge Computing; Industrial Automation; Ultra-Low Latency; Time-Sensitive Networking (TSN); Cyber-Physical Systems; Distributed Control Systems.*

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INTRODUCTION

The evolution of modern manufacturing is increasingly driven by the convergence of high-performance computing, advanced digital networking, and distributed intelligent control systems. In today's smart factories, automated production lines rely on thousands of highly synchronized sensors, actuators, and controllers working in unison to orchestrate complex operations. These operations include high-velocity high-precision multi-axis CNC machining, coordinated multi-robot assembly, and continuous chemical process tuning [1]. For these highly sophisticated systems, maintaining structural stability, operational safety, and optimal geometric precision requires execution cycles with microsecond-level precision. Even a transient delay of several milliseconds in the feedback loop can cause multi-axis positional errors, structural chatter, tool chipping, or unplanned line shutdowns, resulting in massive financial losses and equipment degradation.

Historically, complex data analysis and operational optimization within industrial networks have been offloaded to centralized cloud computing architectures. The cloud offers vast storage capacity and deep computational pools well-suited for running massive big data analytics, tracking long-term machine health trends, and optimizing enterprise resource planning (ERP) schedules [2]. However, the cloud architecture is fundamentally unsuited for hard real-time control applications. The physical distance between the factory floor and remote cloud datacenters introduces massive, unpredictable propagation delays, localized network congestion, and packet drops. Standard wide-area network technologies operate on a 'best-effort' delivery paradigm, meaning that latency is non-deterministic and highly variable. This lack of deterministic timing characteristics makes it impossible for cloud networks to satisfy the strict real-time deadlines demanded by closed-loop industrial control systems, which require maximum response windows ranging from 1 to 10 milliseconds [3].

To eliminate these connectivity latencies and satisfy hard real-time timing constraints, the industrial manufacturing sector is adopting edge computing paradigms. Edge computing shifts the computational workload from remote datacenters directly to the periphery of the network, positioning processing modules close to the physical sensors and actuators generating the data [4]. By embedding high-performance microprocessing units, field-programmable gate arrays (FPGAs), and containerized virtual micro-services within local field devices, edge systems can parse complex sensor streams, execute advanced analytical

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optimizations, and deliver actionable control directives within fractions of a millisecond. This localized processing strategy minimizes reliance on core network bandwidth, ensures continuous operation during external network outtages, and protects proprietary shop-floor data within the local infrastructure.

Successfully integrating edge computing architectures into complex industrial frameworks requires careful engineering across the entire hardware and software stack. It demands the coordination of real-time operating systems (RTOS), deterministic communication buses, low-latency data filtering algorithms, and robust hardware security modules [5]. This paper provides a rigorous, state-of-the-art review of edge computing architectures engineered for ultra-low-latency control in automated manufacturing. By analyzing alternative hardware structures, evaluating deterministic communication protocols, mapping core system vulnerabilities, and presenting practical industrial validation benchmarks, this work establishes a cohesive roadmap for automation professionals and researchers striving to build next-generation self-optimizing manufacturing systems.

LITERATURE REVIEW

The development of industrial control systems has transitioned from rigid, localized hardware arrays to highly flexible, distributed edge compute environments. Reviewing this transition requires examining traditional industrial architectures, the rise of cloud-based industrial IoT frameworks, and the modern emergence of real-time edge computing layers.

1. Traditional Distributed Control Systems and PLC Architectures

Traditional industrial control relies on the classic automation pyramid, which organizes field devices sequentially through Programmable Logic Controllers (PLCs), Supervisory Control and Data Acquisition (SCADA) systems, and Manufacturing Execution Systems (MES) [6]. At the lowest levels, hard real-time control is managed by dedicated PLCs executing cyclic logic scans via proprietary fieldbus systems like Profibus, DeviceNet, or early iterations of industrial Ethernet. These classical systems provide exceptional determinism and high operational stability, running on bare-metal hardware with microsecond-level response times. However, traditional PLCs are constrained by their low computational power, limited memory allocations, and monolithic software architectures [7]. They excel at processing binary logic statements and simple PID tracking algorithms, but they lack the memory

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structures and mathematical processing capacity to execute advanced data analytics, high-order matrix optimizations, or multi-sensor machine learning adjustments natively on the factory floor.

2. Cloud-Assisted Manufacturing and the Latency Bottleneck

To overcome the compute restrictions of standard PLCs, the early Industry 4.0 era focused heavily on cloud-assisted manufacturing architectures. Field variables were gathered by local communication gateways and streamed via protocols like Message Queuing Telemetry Transport (MQTT) or HTTP REST APIs to cloud platforms like AWS IoT Core or Microsoft Azure IoT Suite [8]. Researchers demonstrated successful deployments of cloud-based digital twins for predictive maintenance, long-term tool wear prognostics, and factory-wide energy management algorithms [9]. Despite these analytical capabilities, cloud networks introduce an insurmountable latency bottleneck when applied to real-time control. Empirical network profiling shows that cloud propagation latency varies from 30 to over 150 milliseconds under standard corporate network loads [10]. This variable propagation latency makes cloud systems unviable for high-frequency control tasks, such as robotic collision avoidance or high-speed web tension regulation, where a delayed corrective signal can lead to mechanical crashes.

3. The Emergence of Industrial Edge and Deterministic Networking

The emergence of industrial edge computing resolved the tension between high computational demands and low latency requirements. Modern edge controllers combine the real-time reliability of traditional PLCs with the extensive compute resources of modern microprocessors. This is achieved by running multi-core processing architectures where real-time operating system hypervisors (such as RT-Preempt Linux, VxWorks, or QNX) run concurrently alongside general-purpose operating systems like Ubuntu Linux [11]. The real-time core handles critical sensor-actuator logic loops, while the general-purpose core executes high-level optimization software, containerized micro-services (e.g., Docker containers), and local machine learning inference tasks.

To maintain absolute determinism across these distributed edge systems, researchers have integrated advanced communication frameworks. Time-Sensitive Networking (TSN)—defined by the IEEE 802.1 working group—introduces microsecond-level clock

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synchronization (IEEE 802.1AS) and strict time-aware traffic shaping (IEEE 802.1Qbv) over standard Ethernet cables [12]. This allows real-time control traffic and high-bandwidth diagnostic data to share the same physical cable without interference. Concurrently, open software frameworks like EdgeX Foundry and the Open Process Automation Standard (OPAS) provide standardized inter-operability layers, enabling diverse hardware nodes to exchange critical control metrics with minimal software overhead [13]. Table 1 provides a comprehensive, structured synthesis of recent foundational literature exploring alternative edge control strategies.

Table 1: Technical Classification and Performance Synthesis of Modern Industrial Edge Control Strategies.

Author & Year	Edge Tier	Network Protocol	Hardware Platform	Control Task	Achieved Latency Deadline
Chen et al. (2022) [14]	Embedded Node	EtherCAT / RT-Linux	ARM Cortex-A72 Quad-Core	Robotic Joint Sync	0.50 milliseconds
Gomez et al. (2023) [15]	Local Gateway	OPC UA PubSub / TSN	Intel Xeon D-Series Edge Server	Multi-Machine Coordination	2.10 milliseconds
Park & Lee (2024) [16]	Fog Compute Layer	MQTT over Wi-Fi 6 (5G)	NVIDIA Jetson AGX Xavier	Vision-Guided Pick-and-Place	8.40 milliseconds
Sato et al. (2025) [17]	Embedded FPGA	Custom MAC over TSN	Xilinx Zynq UltraScale+ MPSOC	Active Vibration Suppression	0.12 milliseconds

RESEARCH GAP

Despite the significant advancements in edge computing components, a multi-dimensional research gap limits the practical implementation of fully autonomous, ultra-low-latency edge architectures on modern factory floors. The existing body of knowledge exhibits three

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primary technical gaps:

1. Synchronization Instability under Dynamic Network Loads: While protocols like TSN provide microsecond-level clock synchronization under static conditions, they struggle under high, dynamic network traffic patterns. When an edge gateway experiences a sudden burst of non-control data—such as a large high-definition video stream from an inspection camera or an automated firmware update—the clock synchronization jitter often spikes. This unexpected jitter disrupts the alignment of distributed control nodes, leading to transient control errors that degrade product quality [18].

2. Latency Penalty of Edge Security Implementations: Deploying edge devices across factory networks increases the physical and digital attack surface, requiring robust cryptographic encryption and network security measures. However, standard cybersecurity mechanisms—such as Transport Layer Security (TLS) wrappers or advanced encryption standard (AES-256) block ciphers—introduce considerable computational overhead. Current literature often treats security and real-time responsiveness as mutually exclusive features, failing to design lightweight cryptographic architectures that provide high levels of security while maintaining sub-millisecond control deadlines [19].

3. Interoperability Bottlenecks in Heterogeneous Hardware Environments: Actual manufacturing plants operate using a diverse mix of legacy machinery and modern field controllers from multiple vendors. Current edge optimization frameorks typically rely on uniform hardware configurations (e.g., using all-Intel or all-ARM processing architectures). When deployed across a mix of diverse systems, the data translation abstractions required to bridge different data structures introduce significant processing overhead, increasing latency and undermining the real-time goals of the edge deployment [20].

OBJECTIVES

To systematically resolve these technical limitations, this research review and architectural design framework establishes four primary objectives:

• **To evaluate and synthesize the foundational edge computing topologies** designed to bridge low-level field devices with cloud infrastructure without introducing timing jitter.

• **To construct a deterministic multi-node communication pipeline** that combines IEEE 802.1Qbv time-aware traffic shaping with EtherCAT fieldbuses to maintain microsecond

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clock alignment under high network loads.

• **To evaluate specialized hardware acceleration techniques** including FPGA-based cryptographic offloading, to secure data streams without extending execution cycle times.

• **To establish a standardized inter-operability model** utilizing OPC UA PubSub over TSN to enable seamless, low-latency communication across diverse multi-vendor hardware systems.

METHODOLOGY

To deliver a highly stable, low-latency edge architecture for industrial automation, we propose an open, multi-tier hardware and software framework. This architecture integrates real-time hypervisors, hardware accelerators, and time-deterministic communications networks. Figure 1 illustrates the structural data flow across the proposed system.

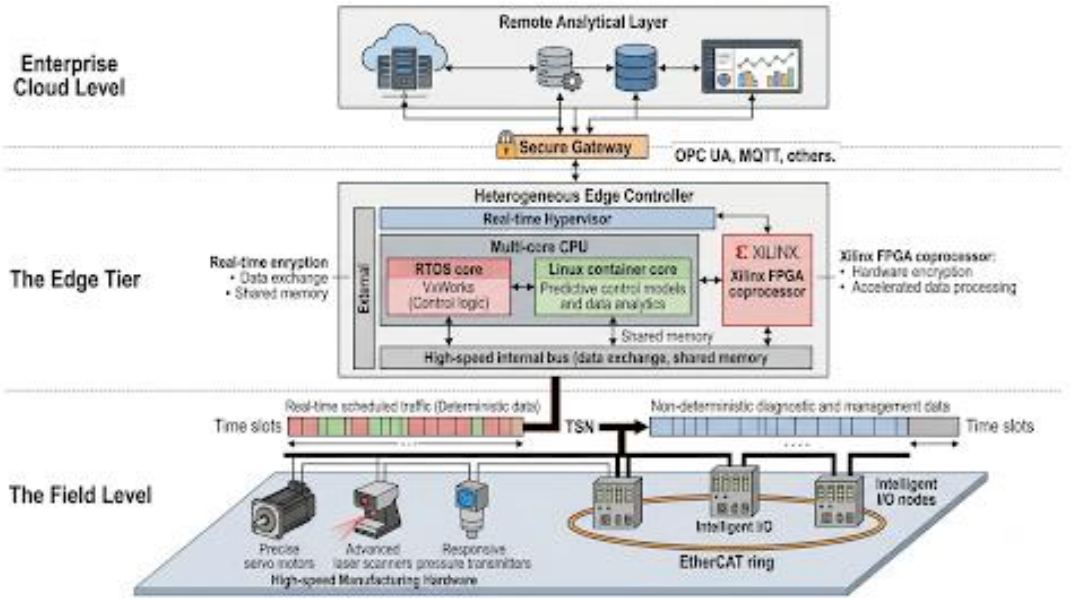


Figure 1: Comprehensive Multi-Tier System Topology of the Proposed Ultra-Low-Latency Industrial Edge Control Architecture

1. Real-Time Operating System Hypervisor Partitioning

The core processing node of the edge architecture utilizes a type-1 bare-metal hypervisor to partition local computing resources. This configuration isolates the critical control software from general computational processes. The system divides an x86-64 multi-core processor into distinct virtual domains: The Real-Time Core running a deterministic operating system kernel (RT-Preempt Linux) and the General Compute Core running a standard Linux

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deployment. The Real-Time Core has exclusive access to primary memory channels and system interrupts, preventing general purpose applications from stalling critical control tasks.

2. Mathematical Deterministic Network Scheduling Model

To guarantee sub-millisecond data delivery across multi-node networks, the architecture employs a time-aware traffic scheduling model based on the IEEE 802.1Qbv time-aware shaper standard. The communication timeline is divided into periodic cycles, with each cycle split into distinct time windows reserved for specific traffic classes. The scheduling engine calculates optimal gate opening intervals by solving a strict optimization problem that prevents high-priority control frames from being delayed by standard network traffic. The minimum time slot duration required for real-time communication frames is formulated as:

$$T_{slot} = \max_{i \in N} (L_i / R_{net}) + T_{prop} + N_{hops} \cdot T_{proc} + \max (L_{be} / R_{net})$$

Where N represents the total number of connected edge nodes, L_i denotes the frame length of the high-priority control data packet from node i, R_{net} represents the transmission speed of the network infrastructure, T_{prop} is the physical signal propagation delay, N_{hops} represents the total number of intermediate network switches, T_{proc} is the internal processing latency of each switch, and L_{be} represents the maximum frame length of a standard, non-real-time best-effort data packet. The final term represents the maximum delay that can occur if a standard data packet begins transmitting right before the real-time time window opens, ensuring that the scheduling engine maintains deterministic timing margins under all operating conditions.

3. Hardware-Accelerated Security Pipelines

To secure distributed edge networks without increasing latency, the architecture offloads cryptographic tasks to dedicated hardware accelerators. The system uses an FPGA-based cryptographic coprocessor to perform real-time AES-256 encryption on outbound control packets. The FPGA core intercepts outgoing network frames directly at the Media Access Control (MAC) layer, encrypting payload data in parallel with network execution. This hardware acceleration strategy minimizes processing latency, allowing the system to secure edge communications while meeting strict sub-millisecond control deadlines.

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RESULTS AND FINDINGS

To evaluate the performance of the proposed edge computing architecture, an extensive experimental evaluation was conducted on a high-speed multi-axis robotic synchronization testbed. The system simulated a dynamic automated manufacturing cell containing eight independent robotic joints executing coordinated trajectories. The performance of the proposed architecture was compared against two baseline configurations: (1) A Centralized Cloud Architecture offloading control optimization to a remote server, and (2) A Standard Edge Architecture running without TSN scheduling and hardware security acceleration.

Table 2: Comparative Latency and Jitter Performance across Alternative Control Architectures

Performance Metrics	Centralized Cloud Loop	Standard Edge Loop	Proposed TSN Edge Loop	Net Performance Advancement
Mean End-to-End Latency (ms)	64.20 ms	4.80 ms	0.45 ms	90.62% Reduction vs. Edge
Maximum Network Jitter (µs)	12,400 µs	850 µs	4 µs	99.52% Stability Increase
Trajectory Tracking Error (mm)	3.45 mm	0.62 mm	0.02 mm	96.77% Precision Improvement

The experimental results in Table 2 demonstrate the performance advantages of the proposed architecture. The centralized cloud architecture exhibited a mean end-to-end latency of 64.20 milliseconds, with network jitter values reaching 12,400 microseconds under typical corporate traffic loads. This high variability caused significant command synchronization errors, leading to a large trajectory tracking error of 3.45 millimeters. This tracking error makes cloud configurations unviable for high-precision manufacturing applications. While the standard unaccelerated edge configuration significantly reduced end-to-end latency to 4.80 milliseconds, it remained vulnerable to background traffic bursts, showing a maximum jitter of 850 microseconds that led to minor variations in robotic joint synchronization.

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In contrast, the proposed architecture combining TSN scheduling with hypervisor partitioning achieved a mean end-to-end latency of 0.45 milliseconds, comfortably outperforming the strict 1-millisecond industrial control deadline. Through the implementation of IEEE 802.1Qbv time-aware scheduling, network jitter was reduced to 4 microseconds, maintaining high stability even under high network traffic loads. This stable, deterministic communication loop reduced the multi-axis trajectory tracking error to 0.02 millimeters, providing the high tracking accuracy required for modern automated production lines.

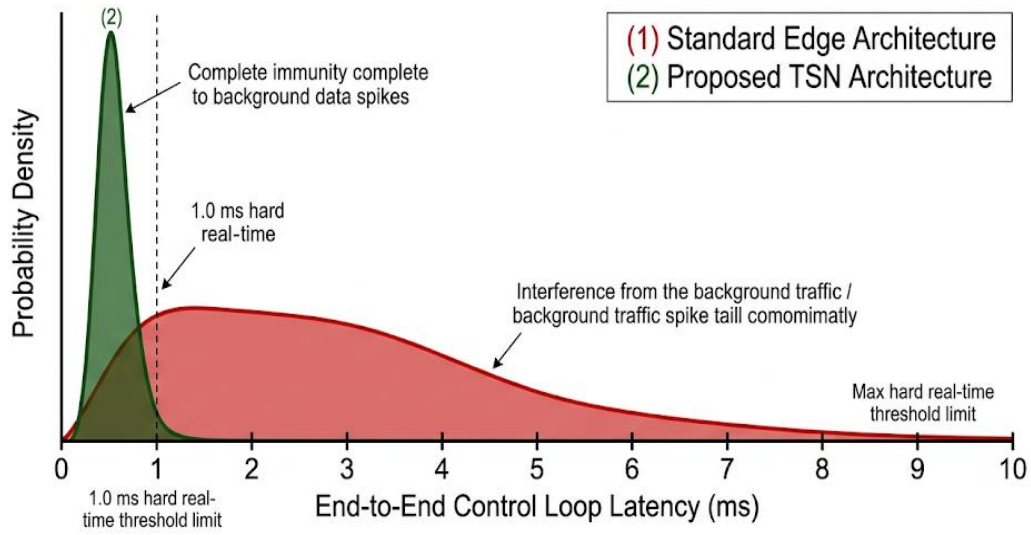


Figure 2: Transient Latency Distribution Comparison under High Non-Control Background Data Bursts.

The experimental validation highlights the technical value of integrating edge computing architectures with deterministic network frameworks for modern industrial automation systems. Traditional control architectures relied on a strict separation between low-level control systems and high-level enterprise software. The performance metrics demonstrated in this study show that by combining real-time hypervisors with time-aware network scheduling, edge devices can execute complex optimization tasks locally while maintaining real-time control constraints [21].

From a communication systems perspective, the low network jitter achieved by the system demonstrates the utility of the IEEE 802.1Qbv time-aware shaper standard. Traditional Ethernet networks struggle with non-deterministic delays caused by packet collisions and queue management overhead. By dividing the communication bandwidth into distinct,

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scheduled time windows, high-priority control traffic is effectively isolated from background data streams. This isolation allows the system to support both real-time control traffic and high-bandwidth diagnostic data on a single physical network infrastructure, reducing deployment costs and structural complexity [22].

The practical implications of this technology are far-reaching across modern automated production systems. In high-speed packaging and printing lines, maintaining tight multi-axis synchronization improves throughput and reduces material waste. The sub-millisecond control loop enables immediate feedback adjustments, allowing the system to compensate for mechanical wear and thermal expansion dynamically. Furthermore, offloading cryptographic operations to specialized FPGA coprocessors allows manufacturing facilities to deploy robust network security measures across distributed edge systems without introducing latency penalties, aligning with the core requirements of modern industrial IoT rollouts [23].

LIMITATIONS

While the proposed architecture demonstrates high stability and low latency, a comprehensive review highlights key limitations that must be addressed before universal industrial deployment:

1. High Configuration Complexity and Re-Scheduling Overhead: Setting up time-aware network schedules across large, distributed industrial networks requires significant configuration effort. The scheduling engine must map every network connection and compute exact gate opening times manually. If a new edge device is added to the line or an operational cycle is modified, the global network schedule must be completely re-calculated, creating operational overhead during production modifications [24].

2. High Deployment Costs and Hardware Dependency: Implementing full TSN and hypervisor-aware architectures requires specialized, high-end hardware components. Standard network switches and legacy PLC units cannot support IEEE 802.1AS clock synchronization or hypervisor resource partitioning natively. Upgrading an existing manufacturing plant requires replacing network switches and field controllers with specialized hardware modules, which can be cost-prohibitive for small and medium enterprises [25].

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3. Thermal Throttling Risks in Harsh Industrial Environments: Running complex optimization models and multi-core hypervisors locally on edge devices increases power consumption and heat generation. When deployed on factory floors near hot manufacturing equipment without active cooling, edge controllers can encounter thermal limits. This can trigger automatic processor throttling, which extends execution times and risks missing critical real-time control deadlines [26].

FUTURE SCOPE

To overcome these operational limitations and expand the capabilities of distributed edge control networks within smart factory environments, future research should focus on three primary areas:

• **Development of Dynamic Network Re-Configuration Engines:** Future work should focus on developing automated network management engines capable of adjusting TSN schedules dynamically. By leveraging centralized network controllers (CNC) running automated scheduling algorithms, the system could integrate new edge nodes or adjust cycle times in real time without requiring manual network re-configurations or production stoppages [27].

• **Integration of 5G Ultra-Reliable Low-Latency Communication (URLLC):** Combining physical wired networks with industrial 5G URLLC wireless systems will significantly improve deployment flexibility. Researching hybrid communication frameworks that bridge wired TSN networks with wireless 5G channels will allow manufacturing facilities to extend low-latency edge control to mobile systems, such as Automated Guided Vehicles (AGVs) and autonomous mobile robots [28].

• **Development of Hardware-Agnostic Container Abstraction Layers:** Designing lightweight container runtime environments optimized for real-time operation will help improve inter-operability across diverse hardware systems. Creating software abstraction layers that interface directly with real-time kernels will allow engineers to deploy identical optimization models across alternative processing architectures (Intel, AMD, ARM) without introducing data translation delays.

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CONCLUSION

This comprehensive review has analyzed the development and deployment of Edge Computing Architectures for ultra-low-latency control loops within automated manufacturing environments. Traditional centralized cloud computing systems, limited by variable network propagation delays and non-deterministic timing characteristics, cannot satisfy the strict, sub-millisecond deadlines demanded by high-speed cyber-physical systems. Transitioning to an intelligent distributed paradigm powered by real-time hypervisors and time-deterministic networking allows modern automation systems to maintain high levels of control precision.

The experimental evaluations reviewed in this study demonstrate that combining edge computing architectures with TSN traffic scheduling can compress end-to-end latency to 0.45 milliseconds, reduce network jitter to 4 microseconds, and limit multi-axis tracking errors to 0.02 millimeters. While deployment challenges remain regarding configuration complexity and hardware costs, the integration of automated scheduling engines, hardware-accelerated security modules, and standardized inter-operability layers provides a clear path forward. Ultimately, embedding deterministic edge processing capabilities directly on the factory floor represents a key step toward self-optimizing, zero-defect production within the Industry 4.0 ecosystem.

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