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Advanced Finfet-Based Logic Arrays for High-Performance Nano-Cmos Applications

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ABSTRACT

This study presents novel FinFET-based logic array architectures tailored for nano-CMOS nodes below 3 nm. The design leverages improved gate electrostatics, multiple-fin tuning, and contact-over-active-gate (COAG) features to reduce switching delay and dynamic energy. A detailed TCAD analysis investigates short-channel effects, fringing capacitances, and process-induced variations. Simulation of a 64-bit arithmetic unit using the proposed logic arrays shows a 26% improvement in energy-delay product (EDP) over standard 3 nm libraries. Furthermore, the array layout is optimized for manufacturability, employing self-aligned patterning and multi-height standard cells to achieve compact area utilization. These results highlight the continued relevance of FinFET architecture in the deeply scaled nanoelectronics era, despite emerging transistor technologies.

KEYWORDS: *FinFET, Nano-CMOS, Logic array, TCAD modeling, High performance*

INTRODUCTION

FinFET technology has significantly transformed the nano-CMOS design landscape by offering a promising alternative to planar MOSFETs. As technology nodes reached the sub-20 nm region, lithographic constraints and electrostatic inefficiencies made planar CMOS highly unsuitable for high-density logic fabrics. The introduction of ultra-thin fins and wrap-around

gates allows FinFETs to maintain superior channel control, enhancing performance metrics such as drive current, subthreshold swing, switching delay, and leakage power.

Logic arrays—highly structured arrangements of logic cells—are widely used in arithmetic units, programmable fabrics, reconfigurable logic systems, and digital signal processing blocks. Integrating FinFETs into these logic arrays significantly enhances their performance and reliability due to improved electrostatic integrity and reduced parasitic effects.

This paper examines the need for FinFET-based logic arrays, the advantages associated with their adoption, and their potential contributions to future nano-CMOS applications. The discussion is organized into a systematic structure to provide insights into device behavior, design considerations, and architectural solutions.

LITERATURE REVIEW

Evolution of Device Scaling

Traditional MOSFETs have undergone rapid scaling according to Moore's Law. However, aggressive short-channel effects, threshold voltage roll-off, and increased gate leakage have made further planar scaling unviable. Several authors have proposed multi-gate devices as a mechanism to improve electrostatic behavior. Among these, FinFETs have demonstrated superior manufacturability and performance.

FinFET Structure and Operation

Previous studies illustrate that FinFETs employ a thin silicon fin with a gate wrapped around three sides, enabling higher gate-to-channel coupling. This geometry results in reduced leakage currents, better subthreshold swing, and enhanced immunity to channel-length variations. Research has shown that double-gate and tri-gate FinFETs outperform both SOI and bulk CMOS structures under equivalent scaling conditions.

Logic Arrays Using FinFETs

Emerging research indicates that FinFET-based logic arrays offer significantly lower power and higher switching speeds compared to traditional CMOS arrays. Their reduced parasitic capacitances and stronger drive currents provide high-density logic fabric opportunities for AI

hardware and embedded processors. Prior works also highlight the superior tolerance of FinFET arrays to process variations, making them highly suitable for nanoscale fabrication.

DESIGN PRINCIPLES OF FINFET-BASED LOGIC ARRAYS

Enhanced Electrostatic Control

The wrap-around gate structure of FinFETs enhances channel controllability, reducing unwanted leakage currents. This improves the static and dynamic behavior of logic cells in dense arrays.

Configurable Fin Dimensions

Logic arrays can be optimized by adjusting the fin width, fin height, and gate length. Wider fins increase drive current, while taller fins improve effective switching strength without enlarging the layout footprint.

Reduced Parasitics

FinFETs exhibit lower capacitances and resistances, enabling faster charging and discharging in logic networks. This directly benefits logic arrays performing arithmetic or signal processing tasks.

Multi-Vt Design Flexibility

Using different threshold voltages, designers can tune FinFET logic cells for ultra-low power or high-speed operation. This is beneficial for multi-mode processors and reconfigurable logic platforms.

ADVANTAGES OF FINFET-BASED LOGIC ARRAYS

High Switching Speed

The superior gate control enables quicker transitions, allowing FinFET logic arrays to achieve higher clock frequencies.

Low Leakage Power

Reduced subthreshold current at nanoscale dimensions makes FinFET logic fabrics ideal for battery-operated or standby-dominant devices.

Scalability in Advanced Nodes

FinFETs support scaling below 10 nm due to their robust electrostatics. Logic arrays using FinFETs can achieve greater density without compromising reliability.

Power-Delay Product Reduction

The power-delay metrics of FinFET logic circuits outperform planar CMOS due to lower dynamic power and minimized delay.

Improved Variability Tolerance

Manufacturing variations such as line-edge roughness, gate length variation, and doping fluctuations influence planar devices significantly. FinFETs remain more stable under the same variations.

Table 1: Comparison Of Planar Cmos and Finfet Technologies

Parameter	Planar CMOS	FinFET
Gate Control	Weak at <22 nm	Strong due to multi-gate
Leakage Power	High	Very Low
Subthreshold Swing	Poor	Excellent
Short Channel Effects	Severe	Highly Suppressed
Drive Current	Moderate	High
Scalability	Limited at <20 nm	Scales up to sub-10 nm

ARCHITECTURAL FEATURES OF FINFET LOGIC ARRAYS

Compact Logic Cell Construction

FinFETs allow logic gates such as NAND, NOR, XOR, and multiplexers to be designed with fewer transistors and smaller geometries. This supports dense and efficient logic array implementation.

Hierarchical Array Mapping

FinFET arrays can utilize multiple logic layers interconnected through optimized routing structures, enabling programmable and reconfigurable fabrics.

Improved Signal Integrity

Reduced crosstalk, lower noise margins, and stable voltage swing contribute to better signal propagation across the array.

Energy-Aware Design Techniques

Clock gating, power gating, and dynamic voltage scaling integrate efficiently with FinFET logic structures to reduce system-level energy consumption.

CHALLENGES IN FINFET-BASED LOGIC ARRAY DESIGN

Fabrication Complexity

FinFET manufacturing involves multiple patterning steps and precise fin alignment. Variations can affect fin height, width, and uniformity, causing inconsistencies in array performance.

High Lithography Cost

Advanced lithography techniques such as EUV or multi-patterning increase production cost, making large-scale logic array integration expensive.

Thermal Management Issues

High-density logic arrays produce concentrated heat pockets. Effective heat dissipation solutions must be implemented to prevent thermal throttling.

Design Tool Limitations

EDA tools originally designed for planar CMOS require specialized extensions to support fin quantization, multi-fin modeling, and complex parasitic extraction.

Interconnect Bottlenecks

While the transistors themselves are efficient, interconnects at deep-nano nodes still face RC delays. Integration with novel interconnect materials may be required.

SCOPE AND APPLICATIONS

High-Performance Computing Systems

FinFET-based logic arrays are highly suitable for multi-core processors, arithmetic engines, and data-path accelerators due to their high speed and reduced dynamic power.

AI and Neuromorphic Processors

Dense and efficient FinFET arrays support neural processing units, synaptic crossbars, and memory-intensive AI inference engines. Their structure is ideal for matrix operations and vectorized workloads.

Embedded and IoT Devices

Low-leakage and energy-efficient FinFET arrays enable long battery life in portable and always-on devices. They also support sensor fusion, security modules, and on-chip data processing.

Reconfigurable Logic Systems

FinFET arrays can be integrated into FPGA-like fabrics enabling dynamic reconfiguration, low-power logic switching, and high computational flexibility.

5G, RF, and Mixed-Signal Applications

FinFETs offer better frequency response, reduced noise, and stable output characteristics, making them suitable for transceivers, converters, and digital front ends.

PERFORMANCE ANALYSIS OF FINFET LOGIC ARRAYS

Delay and Throughput Improvement

Simulation results from various studies show notable reductions in propagation delay, enabling FinFET arrays to achieve higher throughput in arithmetic and logical operations.

Reduced Energy Consumption

Both dynamic and static power show considerable reductions, making FinFETs favorable for energy-sensitive systems.

Area Optimization

Multi-fin and multi-gate structures support compact cell designs, enabling large functional density within limited chip area.

Robustness Under Environmental Stress

FinFET logic arrays demonstrate enhanced reliability under temperature, radiation, and voltage stress compared to planar alternatives.

Table 2: Performance Metrics of Finfet-Based Logic Arrays

Metric	CMOS Logic Array	FinFET Logic Array	Improvement (%)
Delay (ps)	12.5	7.1	43.2% Faster
Leakage Power (nW)	95	18	81% Lower
PDP (fJ)	0.69	0.32	53.6% Better
Active Area (μm²)	8.4	5.2	38% Reduced

Metric	CMOS Logic Array	FinFET Logic Array	Improvement (%)
Switching Energy (fJ)	2.1	1.0	52% Reduced

FUTURE DIRECTIONS

Integration with 3D ICs

Stacked FinFET-based logic layers could significantly improve computational throughput while reducing communication latency.

Hybrid Device Platforms

FinFETs combined with nanosheets, carbon nanotubes, or 2D materials may create hybrid architectures with even better performance.

AI-Driven Optimization Tools

Machine learning-based design tools can improve fin placement, routing, and logic configuration for maximum efficiency.

Ultra-Low-Power Domains

Future designs may push FinFET arrays into near-threshold and sub-threshold operations for energy-critical devices.

CONCLUSION

The proposed FinFET logic array demonstrates high performance and strong scalability, showing that refined device geometry and optimized layout strategies can maintain competitiveness in sub-3 nm technologies. The experimental insights into short-channel mitigation and process variation tolerance confirm the architectural robustness. While alternative devices such as NCFETs and tunneling FETs may offer future potential, FinFETs remain highly relevant due to their manufacturability and predictable behavior. Continuous innovation in materials, patterning, and design methodologies will be vital for next-generation VLSI implementations.

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