

A Noise Reduction Improvement Technique for a Differential Cascode LNA

Digamber Nath Tiwari*, Savita Panday**

Professor, Student***

Department of Electronics and Communication

Acropolis Institute of Research & Technology Indore, SIRT BHOPAL

Corresponding author's email id:digambertiwari@acropolis.in*

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Abstract

A typical common source cascode low-noise amplifier (CS-LNA) can be treated as a CS-CG two stage amplifier. In the published literature, an inductor is added at the drain of the main transistor to reduce the noise contribution of the cascode transistors. In this work, an inductor connected at the gate of the cascode transistor and capacitive cross-coupling are strategically combined to reduce the noise and the nonlinearity influences of the cascode transistors in a differential cascode CS-LNA. It uses a smaller noise reduction inductor compared with the conventional inductor based technique. It can reduce the noise, improve the linearity and also increase the voltage gain of the LNA. The proposed technique is theoretically formulated. Furthermore, as a proof of concept, a 2.4 GHz inductively degenerated CS-LNA was fabricated using TSMC 0.18 μ m CMOS technology. The resulting LNA achieves 1.92 dB noise-figures with the core fully differential LNA at 1.8 V power supply.

Keywords:Low noise amplifier (LNA), capacitive cross-coupling, noise figure, noise reduction, linearity improvement, RF circuit.

INTRODUCTION

Due to the low cost and easy integration, CMOS is widely used to design wireless systems especially in the radio frequency region. The low noise amplifier (LNA) serves as the first building block of the

wireless receiver. It needs to amplify the incoming wireless signal without adding much noise and distortion. The noise performance of the LNA dramatically influences the overall system noise performance. The inductively de-generated

CS-LNA [1]–[5] is widely used due to its superior noise performance. A common gate LNA (CG-LNA) can easily achieve the input impedance matching, but suffers from poor noise performance [6]. The capacitive cross-coupling technique for CG-LNA [7]–[9] partially cancels the noise contribution of the common gate transistor at the output, which improves the noise performance of the CG-LNA. On the other hand, due to the existence of the parasitic capacitance at the source of the cascode transistor, the cascode transistor's noise influences the overall noise performance of the CS-LNA [10]–[14]. In [13], a layout technique to merge the main transistor and the cascode transistor can reduce the cascode transistor noise contribution. Additional inductors can be added at the drain of the main transistor to cancel the effect of the parasitic capacitance, thus improving the noise performance of the LNA [10]–[12] at the cost of larger area for the on-chip inductors.

In this paper, a noise reduction inductor combined with the capacitive cross-coupling technique is proposed to improve the noise and linearity performance of the differential cascode LNA. It can reduce the noise and nonlinearity contributions of the cas-code transistors with a smaller inductor compared with the typical

inductor based technique [10]–[12]. The capacitive cross-coupling technique used in the cascode transistors increases the effective transconductance of the cascode transistors, further improves the linearity of the LNA, and also reduces the Miller effect of the gate-drain capacitance of the main transistor.

Section II describes the basic inductively degenerated CS-LNA, analyzes the noise influence of the cascode transistors, and shows the conventional inductor based noise improvement technique. Section III discusses the original capacitive cross-coupling technique [7]–[9] for CG-LNA, and proposes its application combined with inductor in the cascode transistors of the differential cascode CS-LNA. It also gives the theoretical foundations of the LNA noise reduction with the proposed technique.

BACKGROUND AND PREVIOUS WORK

The LNA noise performance dominates the overall noise performance of the receiver. The inductively degenerated CS-LNA is widely used due to its superior noise performance.

A. Inductively Degenerated CS-LNA

The typical inductively degenerated CS-LNA is shown in Fig. 1, where all parasitic capacitances other than the gate-source capacitances of M_1 and M_2 are ignored for simplicity. It uses an inductor L_s to generate the real impedance to match the input impedance to 50Ω , which results in good noise performance [1]–[4]. If the resistive losses in the signal path, the gate resistance, and the parasitic capacitances except gate-source capacitances are ignored, the overall input impedance of CS-LNA can be simplified to (1), where g_{m1} is the transconductance of M_1 .

$$Z_{in}(S) = SL_g + SL_s + \frac{1}{SC_{gs1}} + g_{m1} \frac{L_s}{C_{gs1}} \quad (1)$$

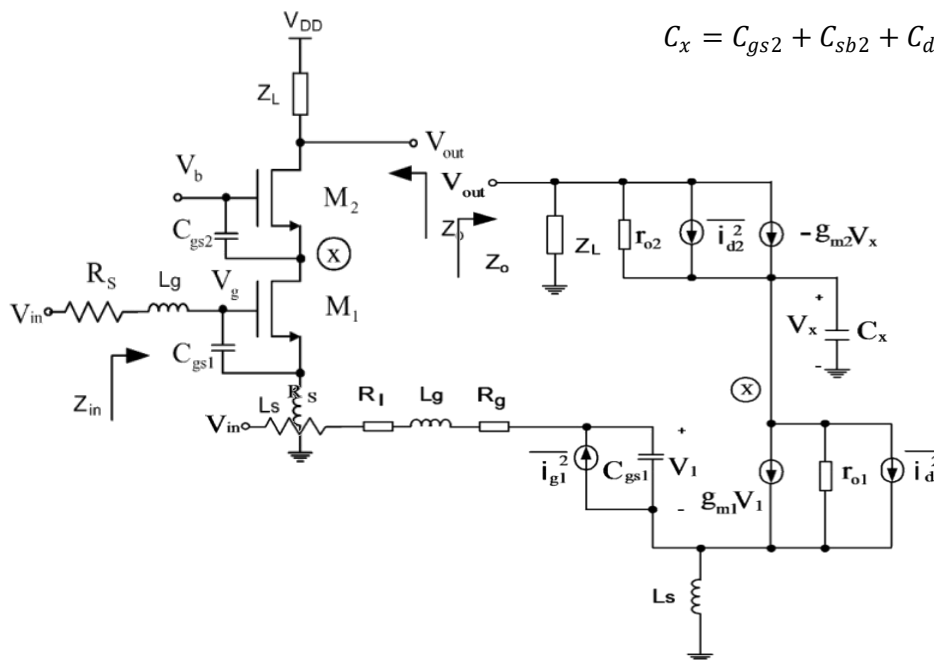


Fig. 2. Small-signal model of cascode CS-LNA for noise analysis

If the noise contribution from the cascode stage is ignored, the noise factor of the cascode CS-LNA becomes [1]

$$F_1 = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \frac{x}{Q_L} \frac{\omega_o}{\omega_T} \quad (3)$$

Fig. 1 Inductively degenerated cascode CS-LNA

The small-signal model of the inductively degenerated cascode CS-LNA is shown in Fig. 2, where C_d and g_{mb} of the transistors are ignored for simplicity. The capacitor C_x represents all the parasitic capacitances at node X. It is estimated as

$$C_x = C_{gs2} + C_{sb2} + C_{db1} \quad (2)$$

$$x = 1 - 2c \sqrt{\frac{\delta \alpha^2}{5\gamma}} + \frac{\delta \alpha^2}{5\gamma} (1 + Q_L^2) \quad (4)$$

$$Q_L = \frac{\omega_o}{R_s} (L_s + L_g) = \frac{1}{\omega_o C_{gs1} R_s} \quad (5)$$

sources of the first stage include the gate induced noise and drain noise sources, but only the drain noise of the second stage is modeled [7]–[11]. From (2) and (7), it can be observed that $\mathcal{C}$ increases the noise factor of the LNA.

$$C = \frac{i_g i_d}{\sqrt{i_g^2 i_d^2}} \cong 0.395j \quad (6)$$

where $\mathcal{R}$ is the input voltage source resistance, $\mathcal{R}$ represents the series resistance of the inductor and R_g is the gate resistance of $\mathcal{M}$. ω_o is the operating frequency, and $\alpha\gamma$, and δ are bias-dependent parameters [1]–[4]. The existence of the parasitic capacitance $\mathcal{C}$ reduces the gain of the first stage, which makes the noise contribution from the cascode stage ($\mathcal{F}$) larger. Thus, the noise factor of the cascode CS-LNA [11] becomes

$$F = F_1 + F_{c\cong} F_1 + 4R_s \gamma_2 g_{do2} \left(\frac{\omega_o^2 C_x}{\omega_T g_{m2}} \right) \quad (7)$$

where $\omega_T = g_{m1} / C_{s1} g_{do2}$ is the zero-bias drain conductance of $\mathcal{M}$ and γ_2 is the bias-dependent factor. Same as in [11], the noise and drain noise sources, but only the drain

noise of the second stage is modeled [7]–[11]. From (2) and (7), it can be observed that $\mathcal{C}$ increases the noise factor of the LNA.

LNA NOISE REDUCTION WITH THE PROPOSED TECHNIQUE

The CG-LNA can achieve wideband input impedance matching, but suffers from poor noise performance. To alleviate this problem, a capacitive cross-coupling technique was proposed in for CG-LNA. It can boost the transistor transconductance with passive capacitors. If the gate-bulk and gate-drain capacitances are ignored, the effective transconductance and input capacitance of the LNA are here derived as:

$$G_{m,eff} = \frac{2C_c}{C_{gs} + C_c} g_{m1} \quad (8)$$

$$C_{in} = \frac{4C_c}{C_{gs} + C_c} C_{gs} = \frac{2G_{m,eff}}{g_{m1}} C_{gs} \quad (9)$$

When $C_g \gg C_s$ the effective transconductance is doubled, and the input capacitance is increased by four times.

The inductively degenerated cascode CS-LNA can be considered as a CS-CG two stage LNA. The CS stage is designed to achieve the input impedance matching and also to obtain best noise performance. The input voltage signal is converted to cur-

rent through the CS transistor. The cascode transistor works as a CG stage. It is designed mainly to reduce the Miller effect of the parasitic gate-drain overlap capacitance in the CS transistor. It also helps to increase the output impedance and to improve the input-output isolation.

An additional inductor L_{add} combined with the capacitive cross-coupling technique is applied to the cascode transistors of the differential LNA to reduce the noise.

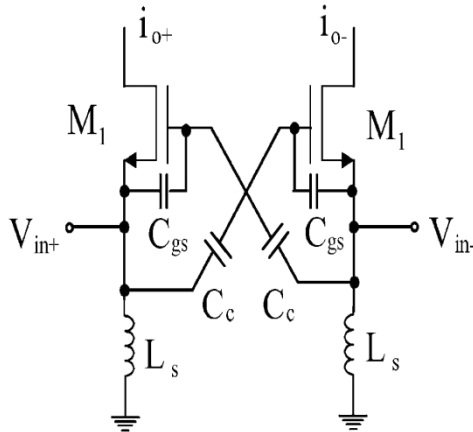


Fig 3 Capacitor cross-coupled differential CG-LNA

The proposed topology is implemented in a fully differential inductively degenerated CS-LNA as shown in Fig. 4. The input admittance at node X is $G'_{m,eff}(j\omega) + jB'_{eff}(j\omega)$ where the effective transconductance of the cascode transistor is expressed as

$$G'_{m,eff} = \frac{2\omega C_c - \frac{1}{\omega L_{add}}}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} g_{m2} \quad (10)$$

Note that in our proposed approach, the cross-coupled capacitors are applied to the cascode transistors. The equivalent input susceptance at node X is not purely capacitive, which can be derived as

$$\begin{aligned} B'_{eff} &= \frac{4\omega C_c}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} \omega C_{gs2} \\ &+ \frac{(\omega C_c + \omega C_{gs2}) \times \left(-\frac{1}{\omega L_{add}}\right)}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} + \omega C_{db1} \\ &+ \omega C_{gd1} + \omega C_{sb2} \quad (11) \end{aligned}$$

where other parasitic capacitances are ignored. From (10), if $\omega C_c \gg \omega C_{gs2}$ and $\omega C_c \gg \omega C_{gs2} - \left(\frac{1}{\omega L_{add}}\right)$ the effective transconductance is doubled and the equivalent susceptance from (11) becomes

$$\begin{aligned} B'_{eff} &= \frac{\omega C_c (4\omega C_{gs2} - \frac{1}{\omega L_{add}})}{\omega C_c + \omega C_{gs2} - \frac{1}{\omega L_{add}}} + \omega C_{sb2} \\ &+ \omega C_{gd1} + \omega C_{db1} \quad (12) \end{aligned}$$

At $\omega = \omega_o$ when (12) equals to zero, the capacitive effect at node X is mainly eliminated, which leads to

$$L_{add} \cong \frac{1}{\omega_o^2(4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})} \quad (13)$$

Using the small-signal model, the noise figure of the cascode LNA yields

$$F' = F_1 + F'_c$$

$$= F_1 + 4R_s\gamma 2g_{do2}\left(\frac{\omega B'_{eff}}{\omega_T G_{m,eff}}\right) \quad (14)$$

Since the effect of the parasitic capacitance at node X is cancelled as

shown in (11)–(13), the noise of the cascode transistors $F_{c'}$, is negligible.

The inductor L_{add} can be implemented with either on-chip Inductor or bonding wire inductor. Its value is reduced by a factor of 4 with respect to the typical inductor based technique [10]–[12].

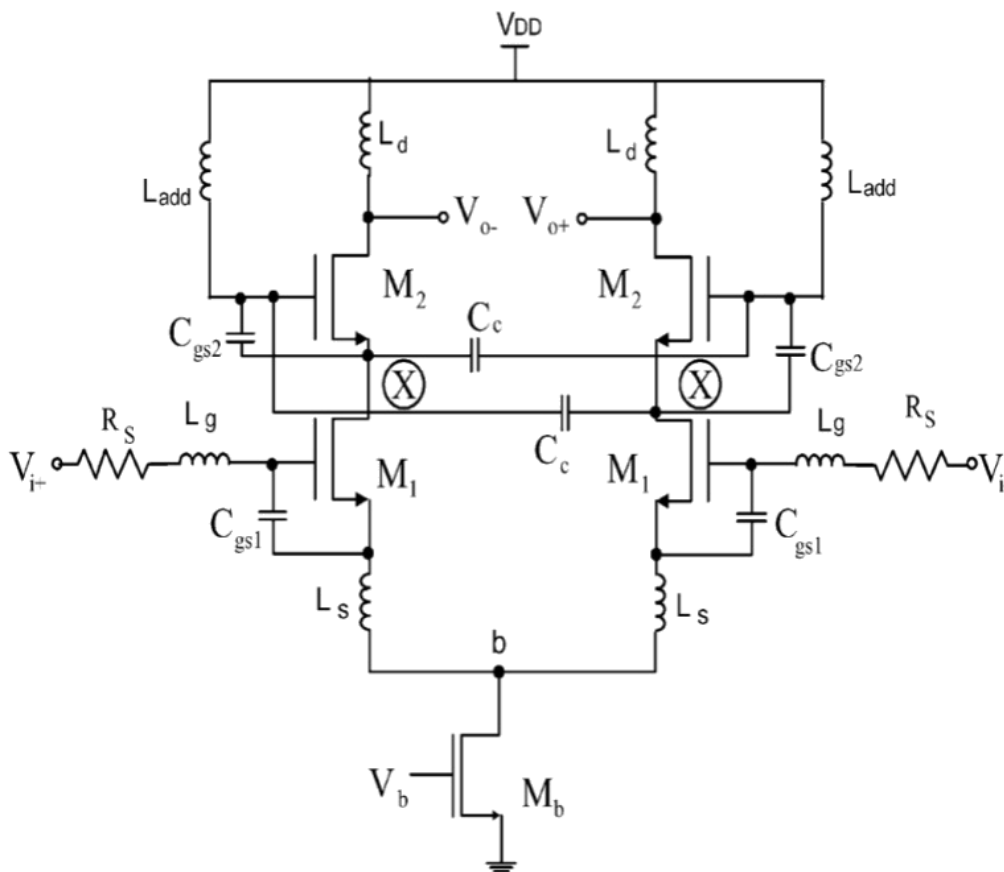


Fig.4. The inductor combined with capacitive cross-coupling technique in a fully differential cascode CS-LNA

Here L_{add} is implemented as a bonding wire inductor. Since now the gates of $\mathcal{M}$ are connected out of the chip using the

bonding wire inductor, it is desired to add ESD protection structures for these pads. In this design, to verify the -posed pro

concept and to get the optimal results, there are no ESD protection structures for these pads. If the ESD protection circuit is used, it can be modeled in first order as a grounded capacitor parallel with the bonding wire inductor. The parallel LC network should be used to replace the L_{add} in the analysis used in this paper.

The proposed LNA topology shown in Fig. 4 is designed with TSMC 0.35 μm CMOS technology and the noise performance is shown in Fig. 5. L is an ideal inductor, while L_s and L_d are on-chip spiral inductors, which are modeled as pi model using ASITIC software [15], [16]. The proposed technique reduces the differential cascode CS-LNA noise figure (NF) by 15.8%, that is from 2.22 dB to 1.87 dB at 2.2 GHz. It will be more significant for the LNAs working at higher frequency.

At the lower frequency, L_{add} short circuited the gates of the cascode transistors to V_D supply (AC ground). In that case, the total capacitive effects at node X in Fig. 4 are not zero and the LNA has worse noise performance. The bonding wire inductance has different PVT values. From (10)–(14), at the operating frequency, we obtain that the variations of G , B , and F can be approximated as

$$\begin{aligned}\Delta G'_{m,eff} &= G'_{m,eff}(L_{add} + \Delta L_{add}) \\ &\quad - G'_{m,eff}(L_{add}) \\ &\cong 0\end{aligned}\quad (15)$$

$$\begin{aligned}\Delta B'_{eff} &= B'_{eff}(L_{add} + \Delta L_{add}) - B'_{eff}(L_{add}) \\ &\cong \frac{1}{\omega_0 L_{add}} \times \frac{\Delta L_{add}}{L_{add}}\end{aligned}\quad (16)$$

$$\begin{aligned}\Delta F' &= F'(L_{add} + \Delta L_{add}) - F'(L_{add}) \cong \\ &\quad 4R_s \gamma 2g_{d02} \left(\frac{\omega_o(4C_{gs2} + C_{sb2} + C_{gd1} + C_{db1})^2}{\omega_T G'_{m,eff}} \right)^2\end{aligned}\quad (17)$$

From (15)–(17), as an example, with 10% variation in L_{add} value, the proposed technique can still achieve around 96% noise reduction for the cascode device, assuming the ideal L_{add} can entirely eliminate the cascode transistor noise contribution. The noise performance of the LNA with varied inductor L_{add} value (from 3nH to 5nH) is shown in Fig. 6. The NF varied from 1.87 dB to 1.95dB that is 4.2% variation for a 67% variation of L_{add} .

The simulation iterations are performed on the capacitor cross-coupled with source degenerated differential LNA circuit to meet design requirements. The simulation wave forms of capacitor cross-coupled with inductively source degenerated

differential LNA operating at 2.4 GHz frequency with supply voltage 1.8 V.

(See Figure:-5)

The simulation iterations are performed on the capacitor cross-coupled without source degenerated differential LNA circuit to

meet design requirements. The simulation wave forms of capacitor cross-coupled without inductively source degenerated differential LNA operating at 2.4 GHz frequency with supply voltage 1.8 V.

(See Figure:-6)

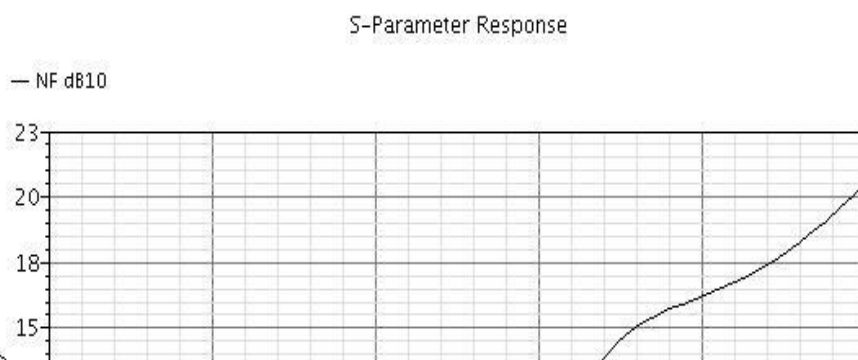
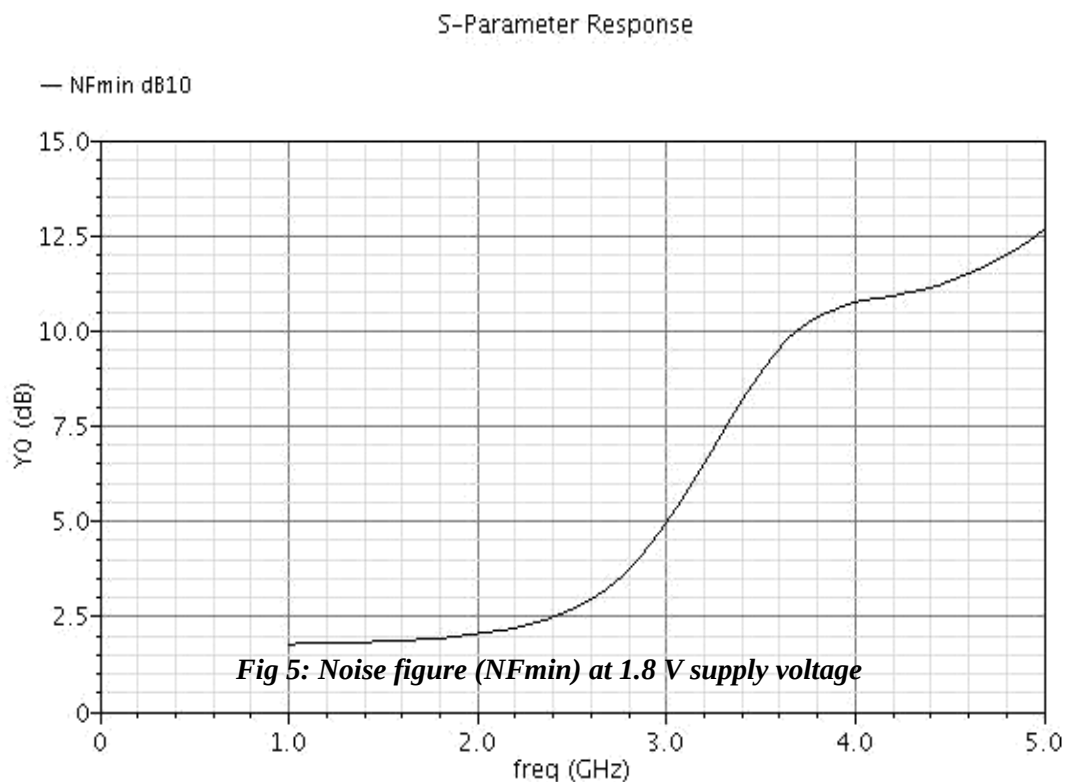


Fig 6: Noise figure at 1.8 V supply voltage

EFFECTS OF THE TECHNIQUE ON THE LNA S11 AND VOLTAGE GAIN

A. Effect on the LNA S11

For the typical cascade CS-LNA C_{gd1} of the transistor M_1 reflects miller impedance at the gate of M_1 . However it is not purely capacitive and its susceptance yields

$$B_{mil1}(j\omega) = (1 + A_v(j\omega)) \times SC_{gd1}$$

$$= \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \frac{L_s}{C_{gs1}} - L_s C_{gs1}}$$

$$\times \frac{1}{g_{m2} + j\omega C_x} \quad (18)$$

Where $A_v(j\omega)$ is the voltage gain from the gate to drain of M_1 . For the proposed LNA, it changes to

$$B'_{mil1}(j\omega) = (1 + A'_v(j\omega)) \times SC_{gd1}$$

$$= \frac{j\omega C_{gd1} g_{m1}}{1 + j\omega g_{m1} \frac{L_s}{C_{gs1}} - L_s C_{gs1}}$$

$$\times \frac{1}{G'_{m,eff} + JB'_{eff}} \quad (19)$$

Where $G'_{m,eff}$ and B'_{eff} are defined, Since the effective transconductance of the Cascade stage increases, the gain of the first stage reduces, Which leads to a reduced Miller effect of C_{gd1} of transistor M_1 . Therefore, the input matching is not very sensitive to the variations of the inductor L_{add} .

B. Effect on the LNA Voltage Gain

Under the input impedance matched condition, the voltage gain of the inductively degenerated cascode CS-LNA can be derived from Figs. 1 and 2.

$$A_v(j\omega)$$

$$= g_{m1} \frac{1}{2R_s \omega_o C_{gs1}} \frac{g_{m2}}{\sqrt{(g_{m2})^2 + (\omega_o C_x)^2}} Z_o$$

$$= g_{m1} Q_{in} Z_o \frac{g_{m2}}{\sqrt{(g_{m2})^2 + (\omega_o C_x)^2}} \quad (20)$$

Where $Q_{in} = \frac{1}{2R_s \omega_o C_{gs1}}$ the quality factor of the LNA is input network and Z_o is the overall output impedance with the proposed technique the cascade CS-LNA gain becomes

$$A_v(j\omega) = g_{m1} Q_{in} Z_o \frac{G'_{m,eff}}{\sqrt{(G'_{m,eff})^2 + (B'_{eff})^2}} \quad (21)$$

$G'_{m,eff}$ and B'_{eff} are defined in equations (10)-(11). The proposed technique increases the overall LNA gain by around 2 dB.

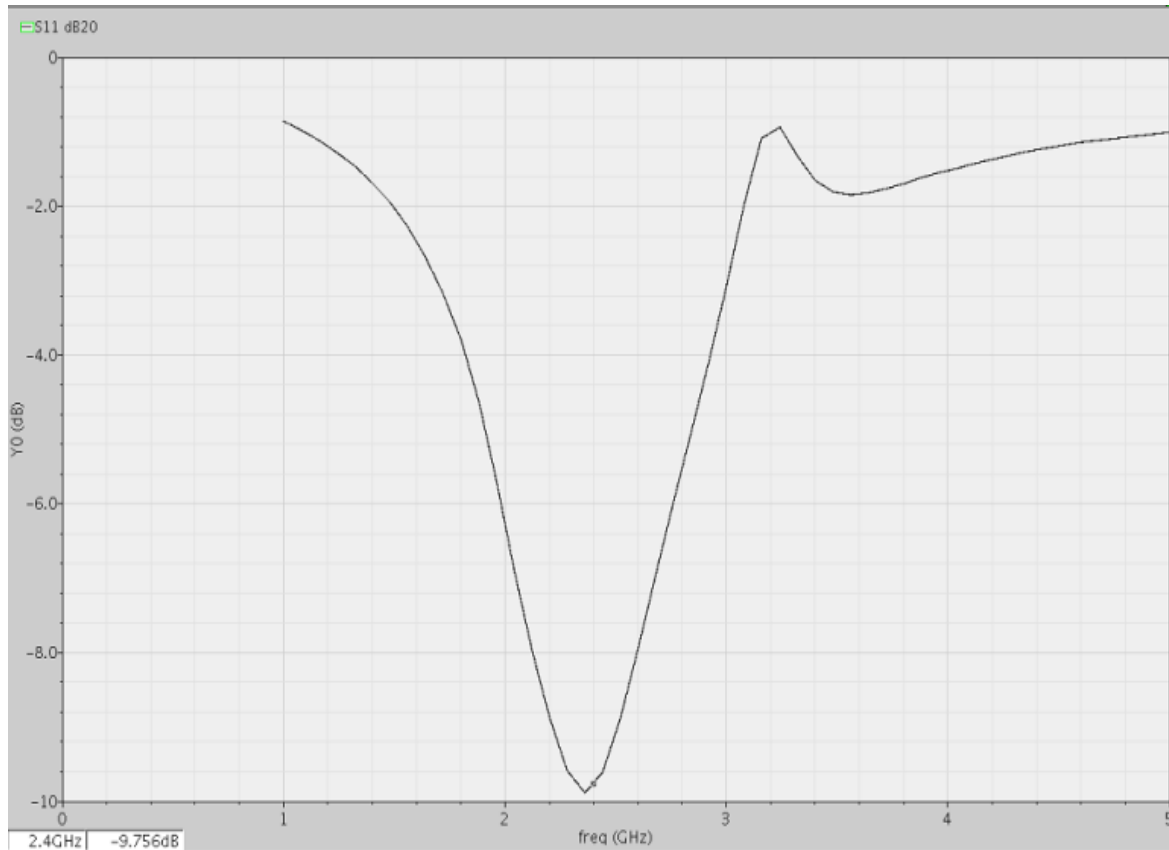


Figure 7: Input matching (S11-parameter) of LNA

SUMMARY OF SIMULATION RESULTS

The various simulation iterations are performed on the capacitor cross-coupled differential cascode LNA circuit to meet

design requirements. The simulation results of capacitor cross-coupled differential cascode LNA and the simulation results of post layout capacitor cross-coupled differential cascode LNA

operating at 2GHz frequency and supply voltages are 1.5 V and 1.8 V. The performance results of simulations are compared to some other standard circuits

reported. The proposed circuit is observed to consume low power in comparison to the existing circuits.

TABLE: 1Performance Comparison with prior published work

Parameters	[24]	[25]	[26]	Simulated	Measured
Frequency (GHz)	2.45	2.46	2.4	2.4	2.4
NF (dB)	2.88	2.36	4.8	1.98	2.2
S11(dB)	<-14.2	<-18.4	<-33	<-13	<-13
Power gain(dB)	12.6	18.9	15.8	21.4	21.2
Power Supply	3	1.8	3.3	1.8	1.8
Topology	Single Ended	Single Ended	Single Ended	Fully Differential	Fully Differential
CMOS Process	250 nm	150 nm	350 nm	180nm	180nm

CONCLUSION

In this paper, a noise reduction and linearity improvement technique for a differential cascode CS-LNA was proposed. The inductor connected at the gate of the cascode transistor and the

capacitive cross-coupling are strategically combined to reduce the noise and nonlinearity contributions of the cascode transistors. It is the first time that the capacitive cross-coupling technique is applied to the cascode transistors of the

CS-LNA. It increases the effective transconductance of the cascode transistor, reduces the impedance seen out by the drain of the main transistor, and thus improving the linearity of the CS stage in the LNA. The inductor resonates with the effective capacitance at the drain node of the main transistor with smaller inductance value compared with the typical inductor based technique. It ideally removes the noise and linearity influences from the cascode transistor, and results in a higher voltage gain. The proposed technique is theoretically formulated.

From simulation results in TSMC 0.35 μ m CMOS process, it reduces the LNA NF by 0.35 dB at 2.2 GHz, and improves the LNA IIP3 by 2.35 dBm. To illustrate the use of the proposed approach in small-size technology, a 10 GHz LNA is also designed using UMC 0.13 μ m CMOS process. The proposed technique reduces the NF from 1.55 dB to 0.95 dB, which is simulated based on the noise model provided by UMC. This verifies the validity of our proposed technique in the deep-submicron process.

REFERENCES

- I. Lin, Y.J. ; Shawn, Y.J. ; Hsu, S.H. ; Jin, J.D. and Chan, C.Y. 2007. 'A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier with Current-Reused Technique'. IEEE Microwave and Wireless Components Letters. 17: 232-234
- II. LIU1, B. ; WANG1, C. ; MA, M. ; GUO, S. 2009. 'An Ultra-Low-Voltage and Ultra-Low-Power 2.4 GHz LNA Design. Radio Engineering'. 18: 527-531
- III. Datta, S.; Dutta, A. and Bhattacharyya, T.K. 2010. 'A Gain Boosted Fully Concurrent Dual-Band Interstage Matched LNA Operating in 900 MHz/2.4 GHz with sub-2dB Noise Figure'. In: International Conference on Communication Control and Computing Technologies. pp. 25-30
- IV. Khurram, M. and Hasan, S.M.R. 2012. 'A 3–5 GHz Current-Reuse g_m -Boosted CG LNA for Ultra wideband in 130 nm CMOS'. IEEE Transaction on Very Large Scale Integration (VLSI) Systems. 20: 400-409
- V. Patil Santosh B , Kanphade Rajendra D 2015. Differential Input Differential Output Low Power high gain LNA for 2.4GHz Applications using 180nm CMOS RF Process IEEE Conference On Computing Communication

- Control And Automation, Vol. 61, No. 9, September 201
- VI. Thomos H.Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, 1998.
 - VII. M.Hella, M.Ismail, "RF CMOS Power Amplifiers: Theory, Design and Implementation", Ohio State University.
 - VIII. S. H. M. Lavasani and S. Kiaei, "A new method to stabilize high frequency high gain CMOS LNA," in Proc. IEEE Electronics, Circuits and Systems Conf., Shadah, United Arab Emirates, Dec. 2003, pp. 982–985.
 - IX. Li, T. Brogan, M. Esposito, B. Myers, and K. K. O, "A comparison of CMOS and SiGe LNA's and mixers for wireless LAN application," in Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2001, pp. 531–534.
 - X. V. Chandrasekhar, "A packaged 2.4 GHz LNA in a 0.15 μ m CMOS process with 2kV HBM ESD protection," in Proc. Eur. Solid-State Circuits Conf. (ESSCIRC), Sep. 2002, pp. 347–350.
 - XI. J. Su, C. Meng, Y. Li, S. Tseng, and G. Huang, "2.4 GHz 0.35 μ m CMOS single-ended LNA and mixer with gain enhancement techniques," in Proc. Asia-Pacific Microwave Conf. (APMC), Dec. 2005, pp. 1550–1553.
 - XII. C. Xin and E. Sánchez-Sinencio, "A GSM LNA using mutual-coupled degeneration," IEEE Microw. Wireless Compon. Lett., vol. 15, no. 2, pp. 68–70, Feb. 2005.

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