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Designing of Efficient Subtractor Circuits using Reversible Logic

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Abstract

*In modern VLSI systems power dissipation is very high due to rapid switching of internal signals. It has been shown that for every bit of information lost in logic computations that are not reversible, KT*log2 joules of heat energy are generated, where K is Boltzmann's constant and T is the absolute temperature at which computation is performed [1]. In fact zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates. The design implemented using Tanner Spice tools*

Keywords: *Reversible gates, CMOS, Fredkin, Toffoli, Peres*

INTRODUCTION

Reversible gates have applications in low power CMOS. A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs.

A reversible logic gate must have same number of inputs and outputs. A reversible gate is balanced, i.e. the outputs are 1s for exactly half of the inputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions. It can realize non balanced functions only with garbage outputs. Some of the major problems with reversible logic synthesis are fan outs cannot be used, and also feedback from gate outputs to inputs is not permitted [9].

Reversible circuits outperform irreversible circuits in terms of power and delay. Subtractors are fundamental building blocks in many computational units. The proposed subtractor is used to

design arithmetic logic circuits for which it is used as fundamental building block. The classical set of gates such as AND, OR and EX-OR are not reversible. The new 3*3 reversible gate called "TR" gate is proposed which is used to design efficient subtractor units [6]. The proposed gate is then used to design half subtractor, full subtractor, and parallel subtractor. The proposed subtractor gives optimized performance with existed in terms of number of reversible gates and garbage outputs and constant inputs. Using TANNER SPICE TOOL, the design was implemented.

THEORY

A. Reversible gates: Reversible logic has become one of the promising research directions in low power dissipating circuit design in the past few years and has found its applications in low power CMOS design, cryptography, optical information processing and nanotechnology [8]. Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions, though it is already briefly described about garbage outputs, in this section that can be defined with more appropriate examples and figures to describe all about reversible logic and reversible logic gates. Garbage is the number of outputs added to make an n-input k-output Boolean function ((n, k) function) reversible. In other sense, a reversible logic gate has an equal number of inputs and outputs (k X k) and all the outputs are not expected. Some of the outputs should be considered to make the circuit reversible and those unwanted outputs are known as garbage outputs. A heavy price is paid for every garbage outputs .[2]

Example: To find out the Exclusive-OR between two variables in reversible computation, the circuit will look like Fig. 1. One extra output should be produced to make the circuit reversible and that unwanted output (P=A, marked as *) is known as garbage.

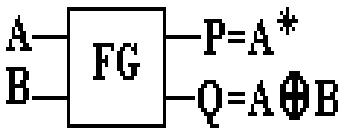


Fig. 1 Reversible Gate

B. Feynman Gate: The most well known (2, 2) reversible gate is the Feynman gate. The logical functions performed by a Feynman gate with input vector (A, B) and output vector (P, Q) are shown in Fig.2. In Feynman gate, one of the input bits act as control signal

(A). That is, if A= 0 then the output Q follows the input B. If A = 1 then the input B is flipped at the output Q. So it is called as controlled NOT (1-NOT) and also called as quantum XOR because of its popularity in the field of quantum computing. This gate is one-through gate which means that one input variable is also output. Feynman gate acts as copying gate when the second input is zero by duplicating the first input at the output.

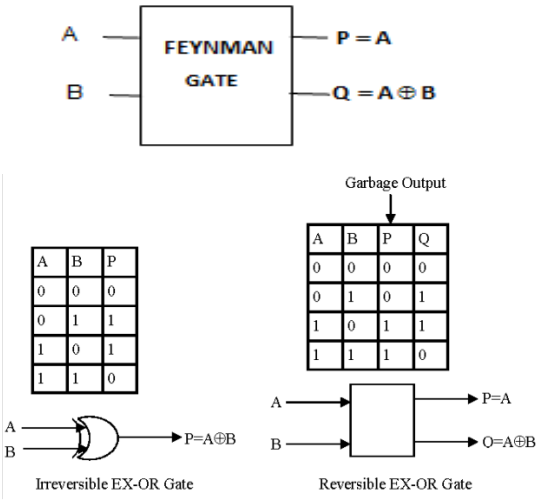
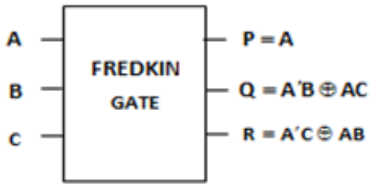


Fig.2. Feyman's Gate and its truth table

C. Fredkin Gate: Fredkin gate, shown in Fig.3, is a (3, 3) reversible gate which realizes P=A, Q=A'B□ AC and R=A'C□ AB where (A, B, C) is the input vector and (P, Q, R) is the output vector. Fredkin gate is also self-reversible as it is its own inverse. It is a conservative gate because the hamming weight (number of logical ones) of an input is same as its output. It uses 'A' as its control input: if A = 0, then the outputs are simply duplicates of the inputs; otherwise if A = 1, then the two input lines (B and C) is interchanged at the output. Fredkin gate is a universal gate, that is, we can construct the basic blocks such as AND, OR, NOT and other gates from this Fredkin gate by pre-setting some of its inputs [4].



D. Tofolli Gate: Tofolli gate is one of the example for (3, 3) reversible gates. Fig. 4 shows the Tofolli gate. This gate is two through gate because two of its outputs are identical with its inputs. Because of this, Tofolli gate is also known as two controlled NOT (2-CNOT). If the first two input bits are one, then the third output bit is the inverse of third input bit i.e., A=B=1, then R = C. Tofolli gate performs basic AND operation when zero is given as its third input (C = 0; R = AB). Any reversible gate has an inverse or dual. The dual of Tofolli gate is also a Tofolli gate and so it is self-reversible [4].

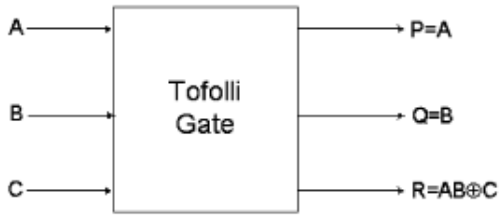


Fig .4.Toffoli gate

E. Peres Gate: Peres gate is another important gate which has a low quantum cost as compared to other gates. It is shown in Fig.5. A single Peres gate can give generate and propagate outputs when the third input C = 0. Because of this, it is quite useful while designing carry look-ahead adders.

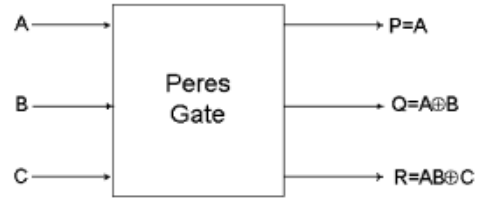


Fig. 5 Peres GATE

F. New Gate: The new gate shown in Fig. 6 is another gate which implements all the basic operations like a universal gate.

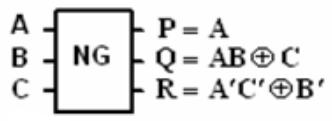


Fig .6: New Gate

G. Double Feynman Gate: The Double Feynman gate shown in Fig.7 is another gate which is also used to implement all basic operations.

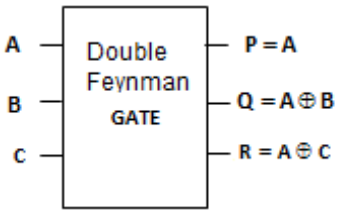


Fig.7. Double Feynman Gate

H. New Tofolli Gate: A 3X3 New Tofolli Gate (NTG) can be defined as Iv=(A,B,C) and Ov=(P=A,Q= A □ B, R=AB □ C) where Iv and Ov are the input and output vector respectively. Fig. 8 shows the block diagram of 3X3 New Tofolli Gate (NTG).

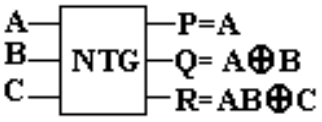


Fig.8. 3X3 New Toffoli Gate

I. TSG Gate: A 4 X 4 one through reversible gate called TS gate "TSG" is developed. The reversible TSG gate is shown in Fig. 9. The TSG gate can implement all Boolean functions. One of the prominent functionality of the TSG gate is that it can work singly as a reversible Full adder unit.

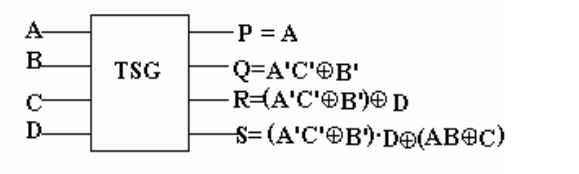
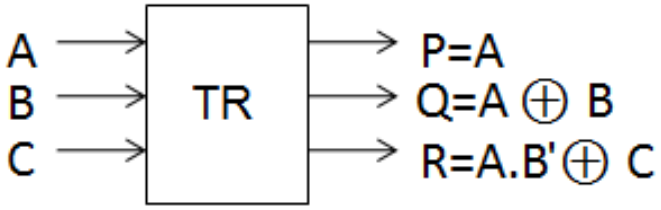


Fig.9. Reversible 4 X4 TSG Gate

G. Proposed 3X3Reversible Gate:

In this section, a 3X 3 one through reversible gate called Proposed gate (TR) is proposed. The proposed reversible TR gate is shown in Fig. 10.The proposed reversible TR gate is a 3 inputs 3 outputs gate having inputs to outputs mapping as (P=A,Q=AEXOR B,R=(A.B')EXORC), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The corresponding truth table of the gate is shown in Table It can be verified from the Truth Table that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed gate can implement all Boolean functions [2]



A	B	C		P	Q	R
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	1	1
1	0	1		1	1	0
1	1	0		1	0	0
1	1	1		1	0	1

Fig.10. Proposed Reversible TR gate and its truth table

Simulation results: The subtractor circuits realized using Proposed TR gate with Standard CMOS logic and simulated with Tanner tools

H. Half Subtractor: The operation described with truth table

Table 3: Half subtractor Truth table

A	B		BORROW	DIFFERENCE
0	0		0	0
0	1		1	1
1	0		0	1
1	1		0	0

The above half subtractor realized with Proposed TR gate shown in Fig.11

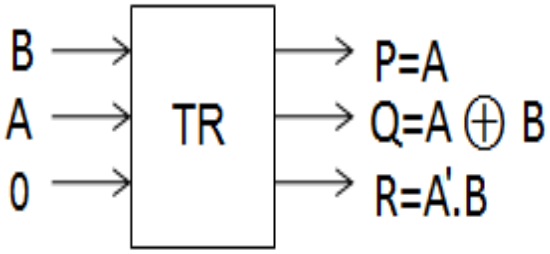


Fig. 11: Proposed TR gate Based Design of Reversible Half Subtractor

Table 4 A comparison of Reversible Half Subtractors

	# OF GATES	**# OF GARBAGE OUTPUTS**
EXISTING CIRCUITS	2	3
PROPOSED DESIGN CIRCUIT	1	1
IMPROVEMENT	50%	66%

The above table.4 shows the result improvement in efficiency through aspects of area, delay and power consumption.

I. Full Subtractor:

To subtract three binary numbers, one can use full subtractor which realizes the operation Y=A-B-C. The truth table of the full subtractor is shown in Table 4.This gives the equation of the borrow and difference as follows:

Diff= A EXOR B EXOR C;

Borrow= A'B EXOR ((A EXOR B)'. C)

Table 5 Truth Table of Full Subtractor

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

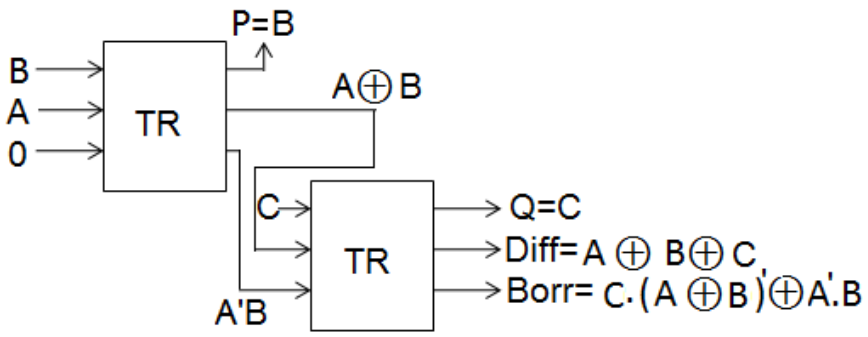


Fig.12. Proposed TR gate Based Design of Reversible Full Subtractor

Table 6 A Comparison of Reversible Full Subtractors

	# OF GATES	# OF GARBAGE OUTPUTS
EXISTING CIRCUITS	5	9
PROPOSED DESIGN	2	2
IMPROVEMENT	60%	77%

J. Parallel Subtractor:

The parallel subtractor subtracts an n bit number Y from an n bit number X. Thus, it can be designed from1 reversible half subtractor (RHS) and n-1 reversible full Subtractors (RFS). Figure 13 shows the proposed reversible design of 4 bit parallel subtractor subtracting4 bit number Y from 4 bit number X (here RHS and RFS refers to reversible half subtractor and reversible full subtractor, respectively, designed from TR gate, g1to g7 represents the garbage outputs). In the design B1to B4 represent the borrow and D0 to D3 represent the difference. Thus using the proposed approach of designing n bit parallel subtractor using the TR reversible gate requires 2n-1 reversible gates, 2n-1garbage outputs and quantum cost of 12n-6. The existing design in literature requires 5n-3 reversible gates, 9n-6 garbage outputs with quantum cost of 17n-11. A comparison between the proposed approach and existing approach in literature is shown in Table 7 for4 bit parallel subtractor.

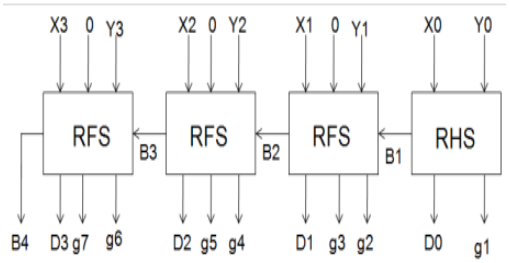


Fig. 15 Proposed TR gate Based Design of reversible Parallel Subtractor

Table 6 A comparison of Reversible Parallel Subtractors

	# OF GATES	# OF GARBAGE OUTPUTS
EXISTING CIRCUITS	17	30
PROPOSED DESIGN	7	7
IMPROVEMENT	64.7%	77%

Sample Layout: All the Gates are simulated and Layouts were also drawn. Proposed gate realized with standard CMOS and its layout are shown in below Fig.16.

CONCLUSIONS

By using reversible logic power dissipation has been reduced drastically. One new reversible TR gate was proposed and by using that gate reversible full subtractor was implemented. The proposed TR gate is being used to design optimized architectures of half subtractor, Parallel subtractor.

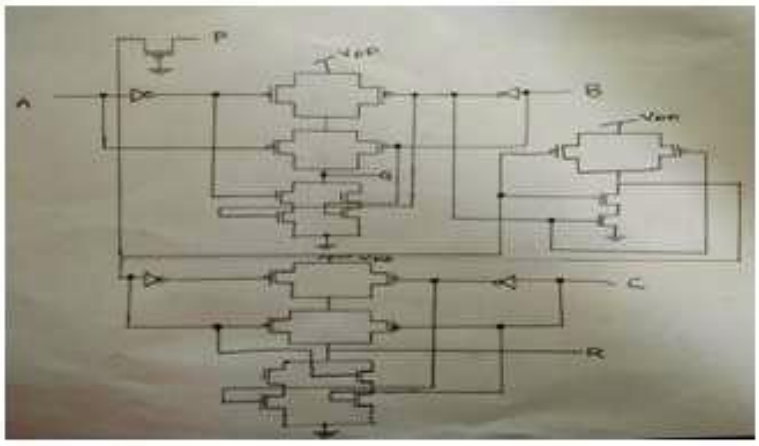


Fig .16(a): Circuit diagram of TR gate

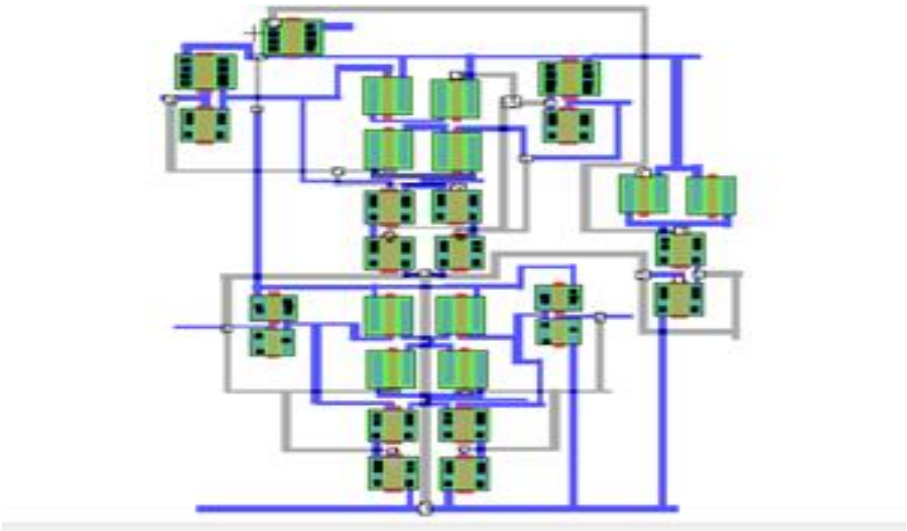


Fig.16 (b) Fig16 Proposed TR gate schematic and its layout

It is proved that the subtractor architectures using the proposed TR gate are better than the existing counterparts in literature, in terms of number of reversible gates and garbage outputs. There are a number of significant applications of reversible logics such as low power CMOS, quantum computing, nanotechnology, and optical computing and the proposed gate (TR) efficient subtractor architectures are one of the contributions to reversible logic. The proposed circuit can be used to design large reversible systems. In a nutshell, the advent of reversible logic will significantly contribute in reducing the power dissipation.

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