MANTECH Publications
International Journal of Research in Electrical, Electronics and Communication Engineering
Volume 4, Issue 1, January-June, 2019

Design of Dual Stack Conditional Push–Pull Pulsed Latches

D. Hadassah Rachel, G.Anjaneyulu

Student, Associate Professor

Department of ECE

MVGR College of Engineering, Vizianagaram, India.

***Corresponding author's email id:-**: rachelbunnie93@gmail.com*

Abstract

The Latches and flip-flops are fundamental blocks for sequential circuits. In this paper, a new type of pulsed latches of is introduced. Its topology is depends on a push–pull final stage driven by two split paths with a conditional pulse generator, which differs in two circuit implementations which can be either shared (CSP3L) or not (CP3L).The concert for proposed topology is very fast and outperforms the familiar transmission gate pulsed latch (TGPL) and TGPL is taken as reference circuit. Hence the proposed pulsed latch has the highest performance yet reported. Accordingly, the proposed class of pulsed latches goes within the current state of the art and it is well suited for VLSI systems that require high performance. The designs are simulated in mentor graphic tools with a supply voltage of 0.8v at 130nm technology.

Keywords: -*Flip-Flops (FFs), pulsed latches, Energy efficiency, energy-delay tradeoff, high speed, low power.*

INTRODUCTION

FLIP-FLOPS (FFs) and latches are ubiquitous elements in CMOS circuits based designs which makes the major portion of the synchronous circuits and, in particular, of both high speed and low energy microprocessors. FFs data-to-output delay (D-Q) and power dissipation affect the processor's clock period and overall power. FFs are part of the clock network, which is responsible for 30%-50% of the whole chip energy budget, and dissipates 80% of clock power. Since VLSI systems are power limited, it is important to reduce the power dissipation in these timing elements as it reduces the overall system power consumption. Energy efficiency of FFs and latches is

even more critical now as speed can be improved only through improvements in energy efficiency of these elements. Thus, Energy-Efficient designs with minimum energy (delay) for a given speed (energy) constraint is crucial.

A variety of push-pull latches have been developed to reduce power consumption and hardware cost [1]. These architectures [1-2] are not suitable for Ultra low voltage applications and also it can make use of additional delay buffers which leads to energy over head. The proposed design eliminates these drawbacks and achieves high performance and low power at approximately same area.

This paper is organized as follows. In Section II, all the FF topologies are presented and a reference circuit TGPL is chosen for comparison with the implemented topology. The main idea and operation of the conditional push-pull pulsed latch is described in Section III, and their detailed circuit implementation in both versions i.e. methodology is discussed in Section IV. In section V the simulated results and comparison with state-of-the-art topologies are mentioned. Conclusions are reported in Section VI.

STATE-OF-THE-ART TOPOLOGIES

To achieve a desired energy-delay tradeoff, various classes of FFs [5] have been proposed depending on the features of the application like high speed, low energy, low standby energy, etc. Selecting the most suitable FF topology for a given application is not a simple task. An appropriate analysis and comparison strategies are applied to compare large number of FF classes and topologies in a 130-nm CMOS technology. Among the state-of-the-art topologies, four existing FF topologies i.e., Transmission gate pulsed latch (TGPL), Transmission gate FF (TGFF), Adaptive coupling FF (ACFF), Skew-tolerant FF (STFF) are studied and a best reference is chosen for comparison The transmission gate pulsed latch Fig. 1 used in various Intel microprocessors is the most energy-efficient FF ranging from high-speed to energy-efficient designs .Only the skew-tolerant FF (STFF) is able to outperform transmission gate flip-flop (TGFF) for extremely high-speed design targets. Hence, although STFF is slightly better than TGPL in terms of pure performance.

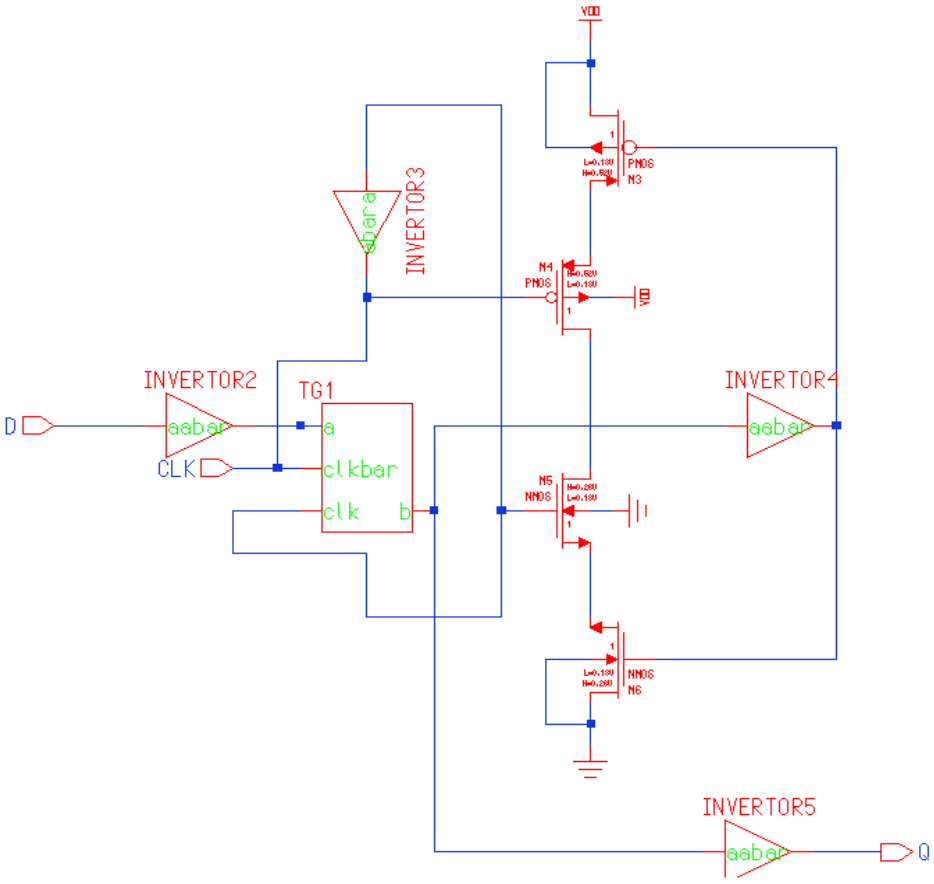

Fig. 1 (a) TGPL topology

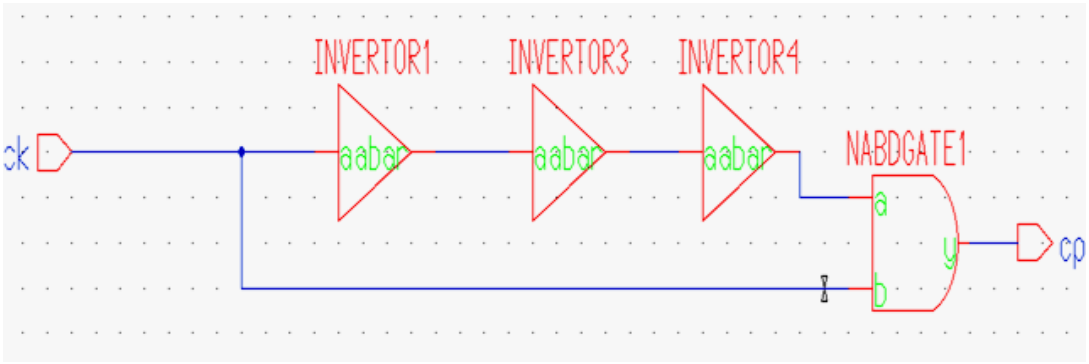

Fig 1(b).Pulse generator topology

Hence, in the following, TGPL will be adopted as a reference for high-speed energy-efficient designs. When slower designs lower design targets are considered, master-slave FFs exhibit better energy efficiency.

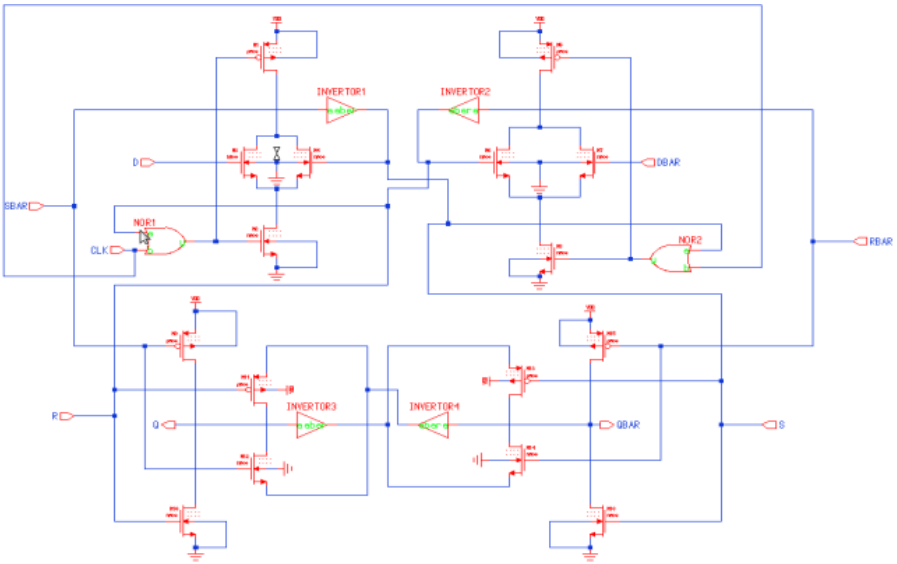

Fig. 2. Skew Tolerant Flip-flop (STFF)

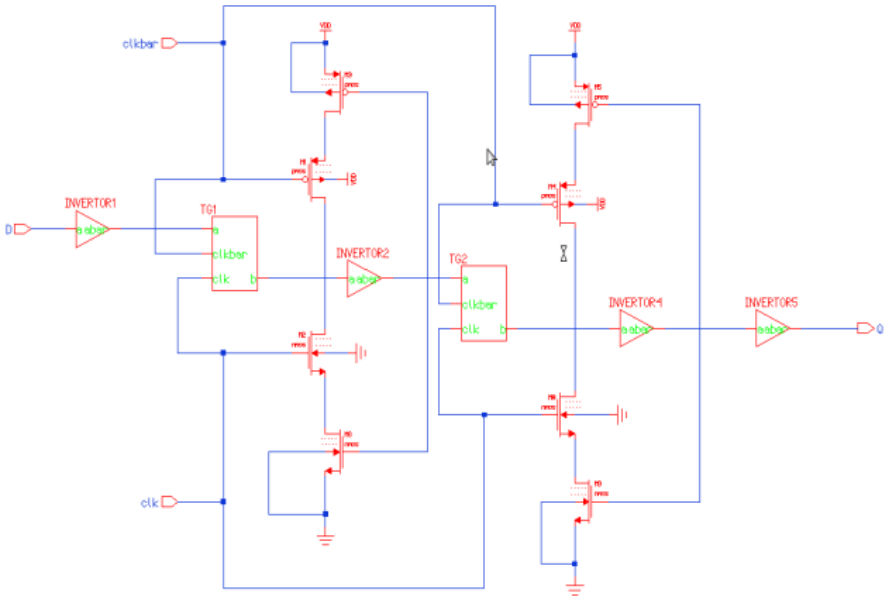

Fig. 3 Transmission Gate Flip-Flop (TGFF)

Among the existing classes of FFs, pulsed latches exhibit the best energy efficiency from moderate to high performance design targets. The transmission gate pulsed latch (TGPL) fig. 1 [7] is the most energy-efficient FF in a large portion of the design space, ranging from high speed to minimum energy-delay (ED) product designs, while simple Master-Slave FFs, TGFF[7] fig. 3and ACFF fig. 4 are the most energy-efficient in the low-power E-D space region[5].

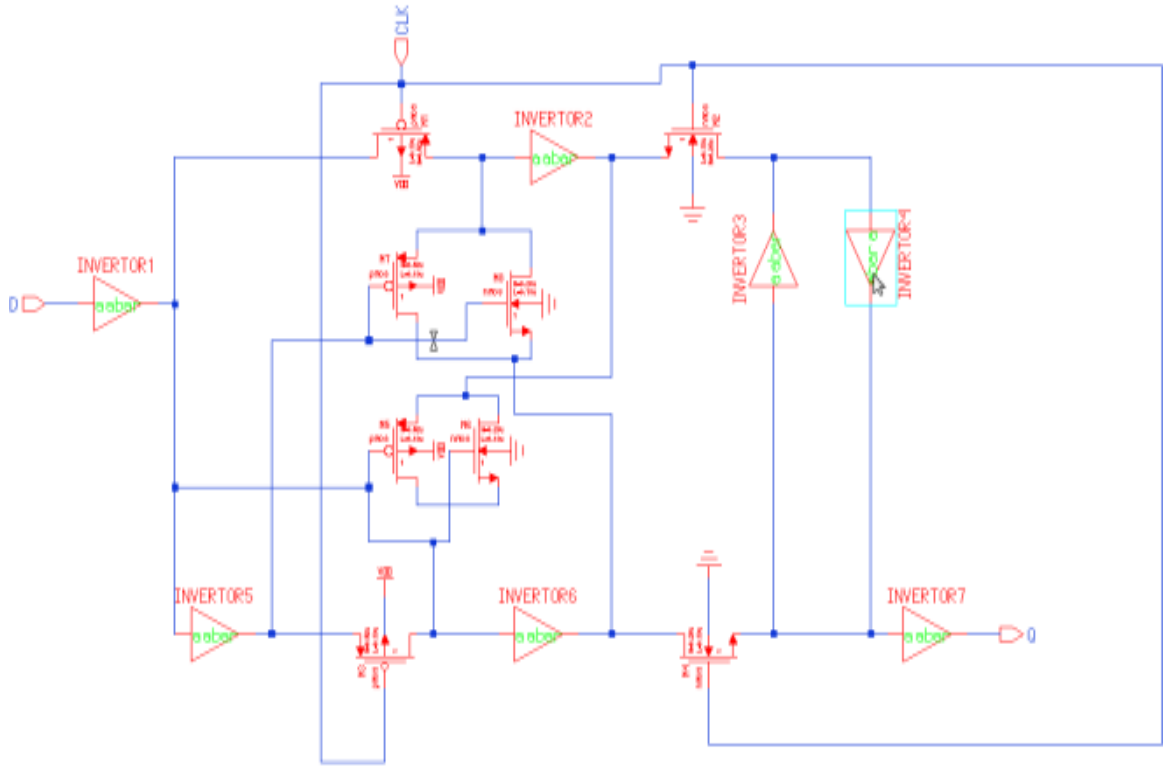

Fig. 4. Schematic diagram of ACFF

TGPL also has the lowest data-in to output (D-Q) delay along with skew-tolerant FF (STFF) (see in fig 2). However, the latter has considerably worse energy efficiency [6]. Hence, the TGPL will be adopted as a reference for high-speed energy-efficient designs.

CONDITIONAL PUSH-PULL PULSED LATCH

The general scheme of the conditional push-pull pulsed latch is shown in the Fig. 5[1]. In order to reduce the delay and make it energy efficient, a push-pull output stage is adopted in its output stage. The push-pull output stage is driven by two split paths that alternatively generate two pulsed signals, active-high reset (R) and active-low set (S). The set and reset pulses are generated after the falling clock edge through the conditional pulse generator in Fig. 5.

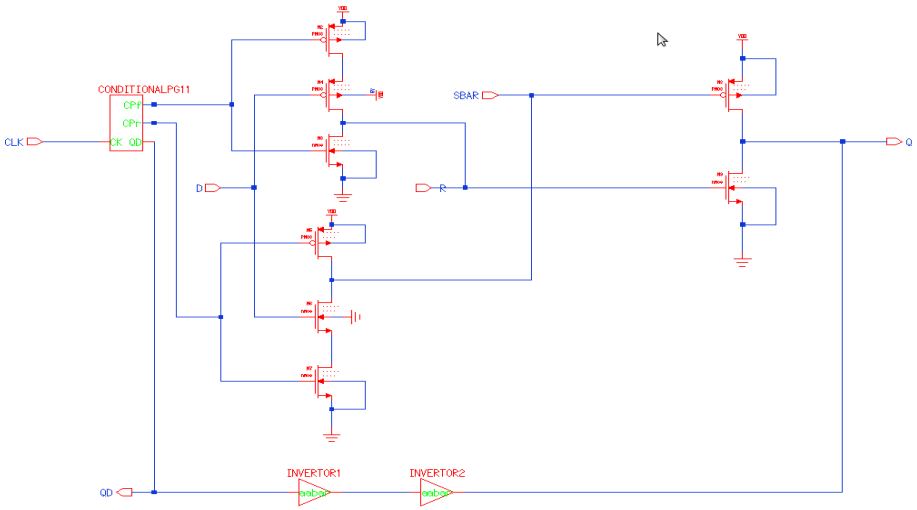

Fig. 5. General scheme of the implemented class of pulsed latch

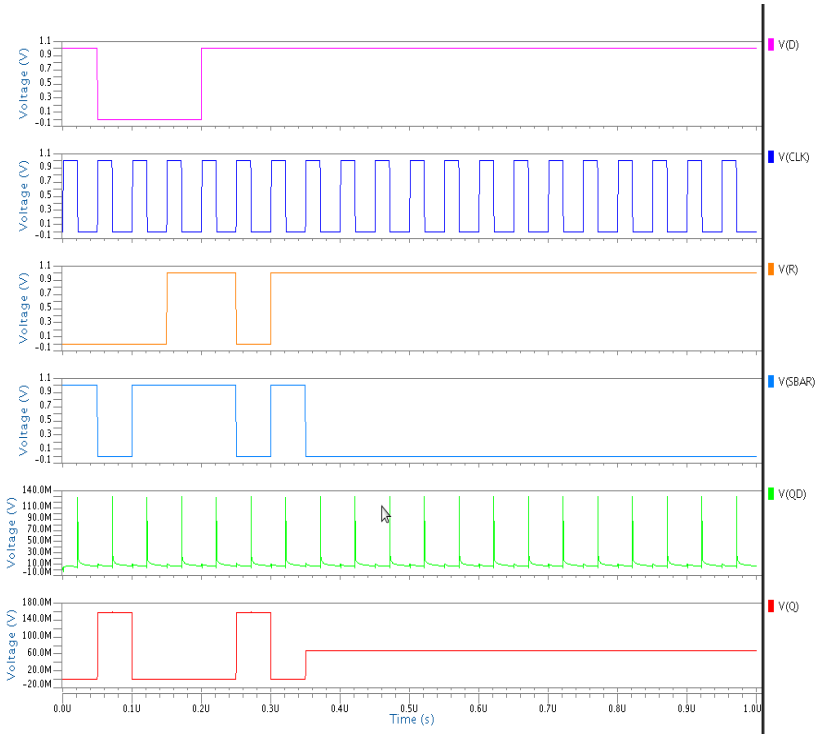

Fig. 6. Waveforms of internal signals of the general scheme in Fig. 7

Fig. 6 depicts the main waveforms of the internal signals. At the falling clock edge (cycle 1 in Fig. 6), the pulse generator checks the previous output QD, whether low or high.

(i) If QD = 1, through CPf, a fall pulse is generated. The rise path is remained unchanged. If D=1, half latch M4-M6 is disabled and R retains its previous value. And if D = 0, the M1–M3 half latch is enabled, and a high pulse

(R) is generated in fall path. Thus making M7 in output stage ON and the output Q is pull down.

(ii) (ii) If QD= 0, through CPr, a rise pulse is generated. Fall path is unchanged. If D = 0, the latch M4–M6 is disabled and keeping S high. If D = 1, the latch M4–M6 is enabled and the CPr pulse pulls down S by turning M8 ON and output, Q is high.

METHODOLOGY ----- IMPLEMENTATION OF CONDITIONAL PUSH-PULL PULSED LATCH CONCEPT: CP3L AND CSP3L TOPOLOGIES

The novel pulsed latch in Fig. 5, in which critical path is lightly loaded to meet optimum speed and power product can be implemented in two versions, respectively, without (Section IV-A) and with (Section IV-B) shareable pulse generator.

(A). CP3L : Conditional Push-Pull Pulsed Latch:

The Conditional push-pull pulsed latch (CP3L) is depicted in Fig. 7. The output Q is driven by a keeper circuit (M9–M12 in Fig. 7). When R = 1 the pull-down transistor of the output stage, M7 is ON and the pull up network of the keeper through M11, is OFF. Similarly, if S=0 the pull-up transistor of the output stage, M8 is ON and the pull-down network of the keeper through M10, is OFF. The pulse generator in CP3L comprises a clock phase generator, a pseudo-NAND for the fall path (M15-M19) and a pseudo-NOR gate for the rise path (M20–M24).

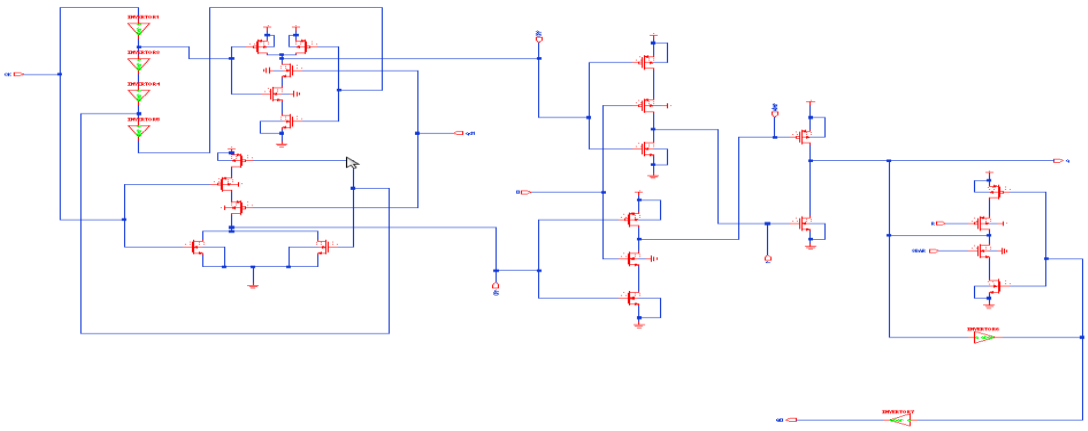

Fig.7. CP3L topology (area in dashed line is shareable among multiple cells).

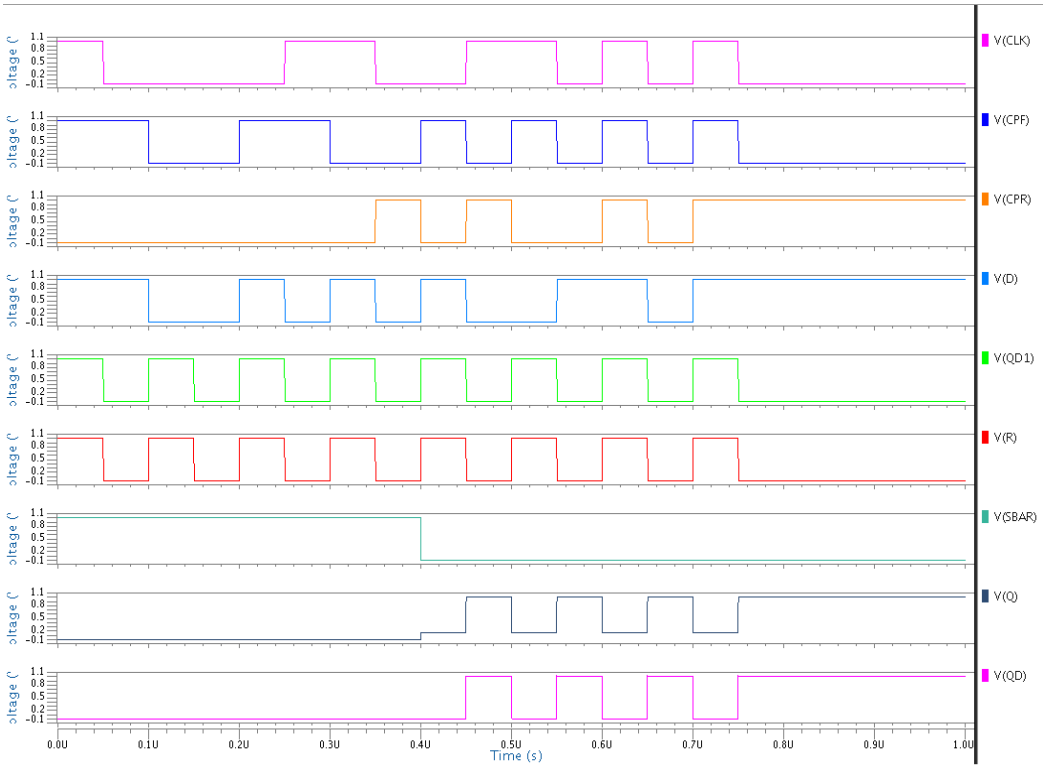

Fig7(a):simulated waveforms for CP3L

D=1(0). By delaying the previous output, power dissipation is reduced due to the elimination of undesired transitions on $CP_f$and CP_r.

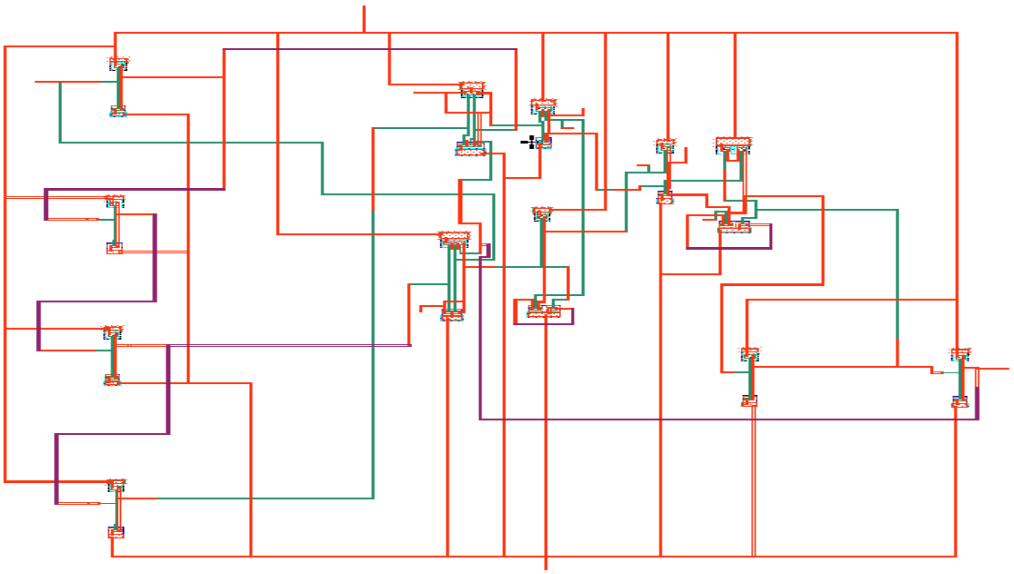

Fig7 (b): layout of conditional push pull pulsed latch

B). CSP^{3}L : Conditional Shareable Push-Pull Pulsed Latch:

The Conditional shareable push-pull pulsed latch (CSP^{3}L) is depicted in Fig. 8.In CP^{3}L, the pulse generator cannot be shared among different latches since pseudo-NOR/NAND are driven by Q_D, which is unique for each latch. In CSP^{3}L, by integrating the conditional logic in the latch, the pulse generator can be shared among several flip-flops within the chip. In CSP^{3}L, static NAND/NOR gates are used in the shareable pulse generator to generate the pulses $CP_{f,ext}$ and $CP_{r,ext}$ which can be distributed to different latches requiring the same role as CP_f and CP_r in CP^{3}L.

For this purpose two transmission gates and few keeper circuits have to be added at the pulsed nodes. Two more inverters are added in the delay stage in feedback path than in CP^{3}L, as the transmission gates in static NOR/NAND needs complementary control signals.

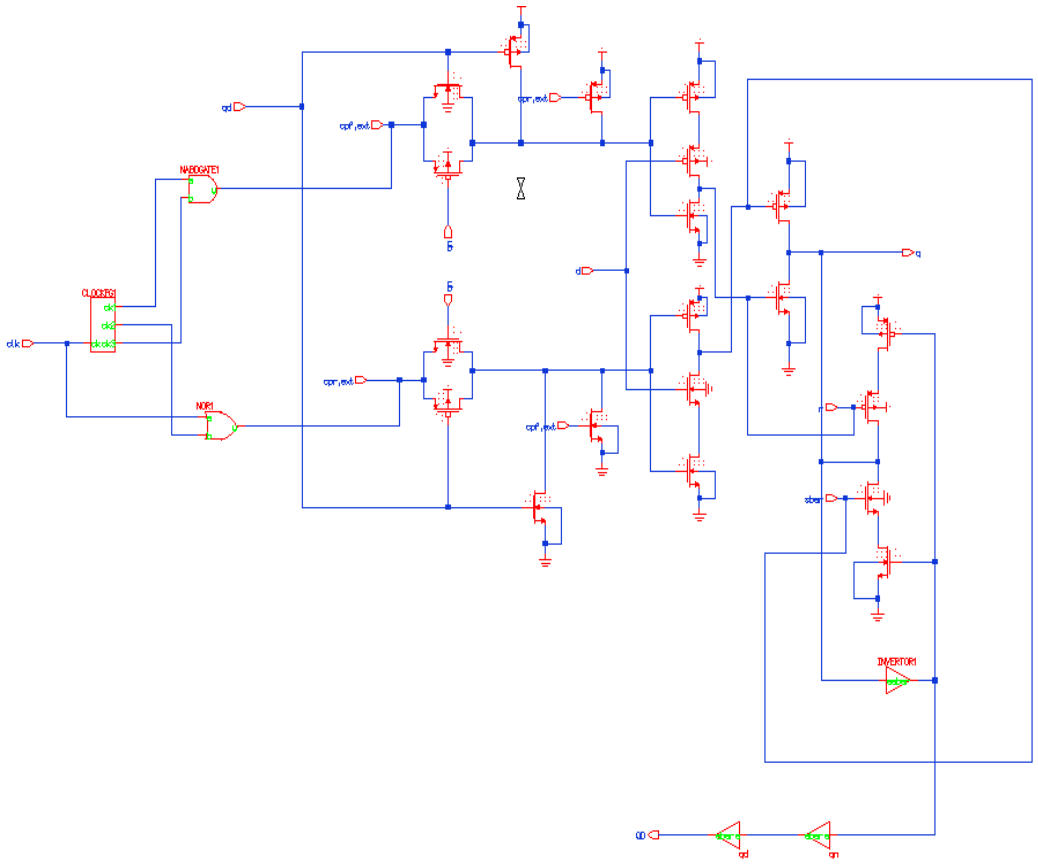

Fig. 8 CSP^{3}L topology (area in dashed line is shareable among multiple cells).

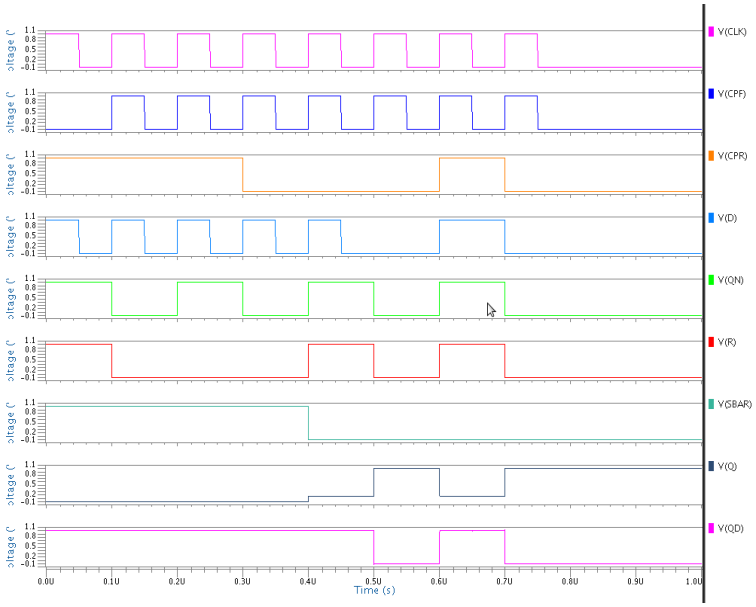

Fig8(a):simulated waveforms for CSP3L

SIMULATION RESULTS

Comparison of State-of-art-topologies

The below are the tabulated results of the existing state-of-art-topologies namely TGPL, TGFF, ACFF, STFF, CP3L, CSP3L, DSCP3L, DSCSP3L.

Table. I give the results of topologies which are simulated in 180nm technology, and its average power, clock delay and energy was observed.

Table. I Comparison of different state-of-art- topologies using 180nm technology

Flip-flop Topologies	**Average Power (Watts)**	**Clk- Q Delay (seconds)**	**Energy (Joules)**
STFF	92.518 µ	49.167N	4.548pJ
ACFF	28.028 µ	101.005N	2.830pJ
TGFF	3.8199N	798.88p	0.030fJ
TGPL	94.776 µ	22.120N	2.096pJ
CP^3L	299.07µ	240.39p	0.718pJ
CSP^3L	204.198µ	237.98p	0.485pJ
$DSCP^3L$	115.538µ	99.87N	11.537pJ

DSCSP^{3}L	11.63µ	1.591N	18.503fJ

Table. II Comparison of different state-of-art- topologies using 130nm technology

Flip-flop Topologies	**Average Power (Watts)**	**Clk- Q Delay (seconds)**	**Energy (Joules)**
STFF	115.5390 µ	48.610N	5.616pJ
ACFF	27.0287µ	51.0N	1.378pJ
TGFF	3.6051N	735.67p	0.026fJ
TGPL	2.558 N	154.30p	0.0394fJ
CP^{3}L	237.5 µ	213.40p	0.5068pJ
CSP^{3}L	161.402 µ	210.39p	0.3395pJ
DSCP^{3}L	92.518µ	99.83N	9.236NJ
DSCSP^{3}L	192.45µ	1.35N	2.598NJ

Table. II gives the result of topologies which are simulated in 130nm technology and the two versions of conditional pulsed latches are simulated and their results are compared with the reference flip-flop.

CONCLUSION

A novel class of pulsed latches has been introduced in this paper. Its push–pull final stage and split paths in the first stage enable a significant reduction in power and parasitic delay effort. The energy efficiency of the proposed pulsed latches enables a significant improvement beyond the state of the art. Finally, the CP^{3}L and CSP^{3}L were shown to be equivalent in terms of energy and performance, hence both topologies are equally worth considering when designing highly energy efficient systems. The choice between CP^{3}L and CSP^{3}L is driven by preliminary design decisions on the clocking scheme Indeed, CP^{3}L does not allow for sharing a pulse generator, but has lower area than CSP^{3}L if the pulse generator is included.

REFERENCES

I. Elio Consoli, Gaetano Palumbo, \ Jan M. Rabaey, and Massimo Alioto, "Novel Class of Energy-Efficient Very High-Speed Conditional Push–Pull Pulsed Latches" Ieee Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 7, July 2014.

II. T. Fischer, S. Arekapudi, E. Busta, C. Dietz, M. Golden, S. Hilker,A. Horiuchi, K. A. Hurd, D. Johnson, H. McIntyre, S. Naffziger, J. Vinh,J. White, and K. Wilcox, "Design solutions for the Bulldozer 32nm SOI 2-core processor module in an 8-core CPU," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 78–80.

III. M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I—Methodology and design strategies," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 5, pp. 725–736, May 2011.

IV. S. Naffziger and G. Hammond, "The implementation of the next generation64b itanium microprocessor," in Proc. IEEE ISSCC,Feb. 2002, pp. 276–504.

V. Research Inventy: International Journal Of Engineering And Science Vol.4, Issue 10 (October2014), PP 06-10. "Improved Power Gating Technique for Leakage Power Reduction".

VI. P. Gronowski, W. Bowhill, R. Preston, M. Gowan, and R. Allmon, "High-performance microprocessor design," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 676–686, May 1998.

VII. B. Dally,"Architectures and circuits for energy-efficient computing," inProc. CICC, pp. 1–10.Sep. 2012,

VIII. D. Bailey and B. Benschneider, "Clocking design and analysis for a600-MHz alpha microprocessor,"IEEE J. Solid-State Circuits, vol. 33, no. 11, pp. 1627–1633, Nov. 1998.