

Sigma-delta ADC Design for Wireless Applications at One Bit

Abhinav VS

Student

Department of ECE

NSS College of Engineering, Palakkad

Corresponding Author's Email: 008145abhinav@gmail.com

Abstract

In this project, a 1st order single-loop single-bit digital sigma-delta modulator is designed. In this project, a 1 bit ADC is used in conjunction with a Difference Amplifier, integrator, and DAC in feedback. As an ADC, a two-stage comparator is employed. Because of this design of anti aliasing filter, oversampling and noise shaping technologies are used. Tanner is also used to validate the design's behavioural simulations. A top-down system design technique is offered to estimate the degree of effect of modulator structural factors on modulator performance. This technique not only gives crucial guidance for implementing the modulator in an FPGA processor, but it also decreases design complexity and shortens the integrated circuit (IC) design time.

Keywords: *FPGA, DAC, ADC, Sigma-Delta modulator, Oversampling*

INTRODUCTION

The most common type of analog-to-digital conversion utilised in audio applications is sigma-delta modulation. It's also utilised in D/A converters and sample-rate converters. The easiest way to understand sigma-delta modulation (SDM) is to compare it to classic pulse-code modulation (PCM). Typically, a PCM

converter samples an input signal at the Nyquist frequency and generates an N-bit version of the original signal. This approach, however, necessitates the quantization of 2^N levels. High resolution in PCM conversion is difficult to achieve due to the necessity to properly represent numerous quantization levels and the resulting circuit complexity, whether

achieved via consecutive approximation registers, pipelined converters, or other approaches. This is the driving force behind sigma-delta modulation. Figure 1 shows a block schematic of the Sigma Delta Modulator.

Sigma-delta modulators are one-bit systems. This modulator employs a one-bit ADC to transform analogue input into a one-bit binary representation. As seen in the accompanying figure, the Block Diagram of the Sigma Delta Modulator consists of a Difference Amplifier and an Integrator. A feedback DAC is used to transform a 1 bit binary representation into an analogue signal, which is then fed as input to the Difference Amplifier through negative feedback, increasing the circuit's. Delta Sigma modulation requires

oversampling techniques to provide a high signal-to-noise ratio, which means that the analogue signals is sampled at a rate many times faster than the Nyquist rate.

METHODOLOGY TO BE EMPLOYED

The Design Methodology of Sigma Delta Modulator given below. It consists of various steps to find the output data. In this, a ADC generate the code depending on the input. It consists of various parts such as Difference Amplifier and Integrator. In feedback DAC is used which convert 1 bit binary representation into analog signal which will be applied as input to the Difference Amplifier using negative feedback which increases the stability of the circuit.

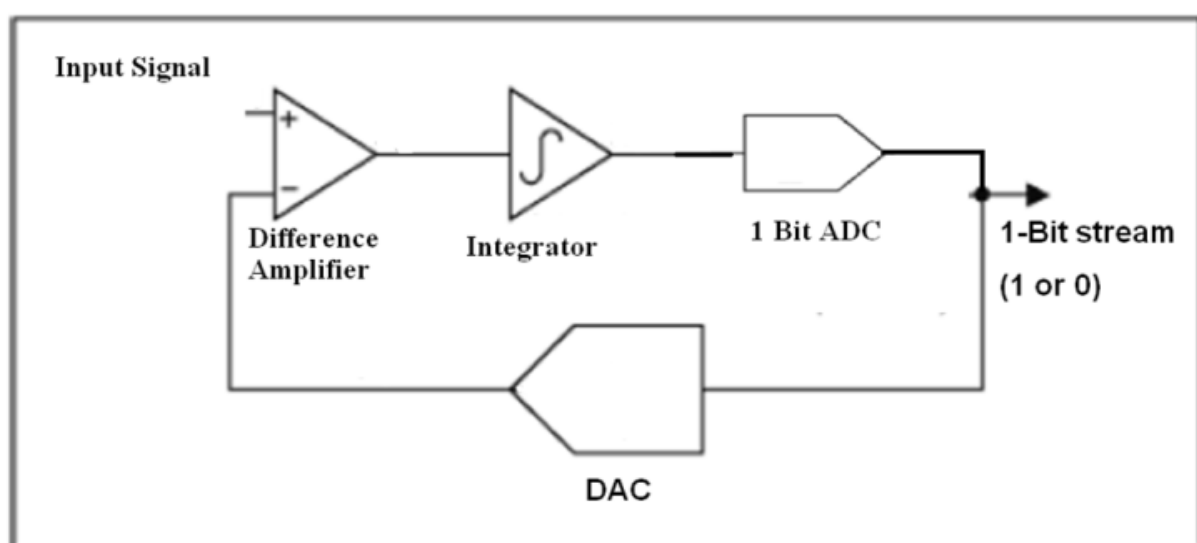


Figure1:- Block Diagram of sigma Delta modulator

OVER SAMPLING AND NOISE SHAPING

a) Oversampling

Normally sampling frequency is twice the frequency of input signal for proper sampling and avoiding the aliasing effect

and to reconstruct the original signal at the receiver. When we use sampling frequency very high than input signal frequency then that type of sampling is called as “Oversampling”.

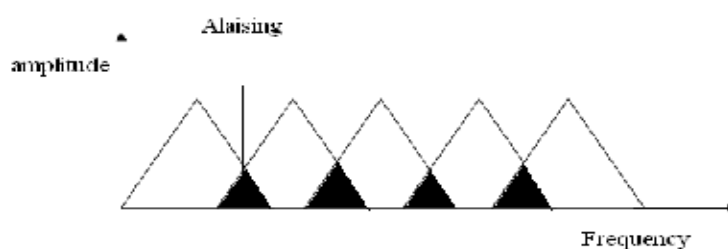


Figure 2: under sampled Signal

If we oversampled the signal then Aliasing can be removed and quantization noise of the circuit reduces. Over sampling ratio of 128 is used the above circuit.

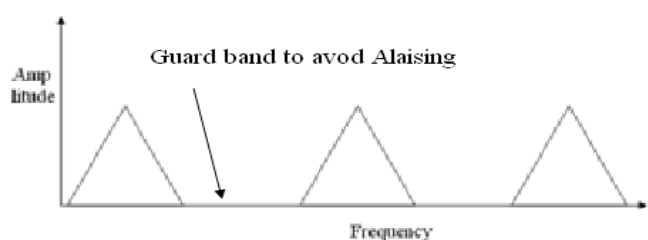


Figure 3: Over Sampled Signal

As signal is oversampled then SNR increase as stated above. The relation between Over sampling rate and modulator performance is shown in table below:-

Table 1: The Relationship between Over-Sampling Rate and Modulator Performance

Over Sampling Rate	SNR	No. of significant bits
16	82	13
32	102	17
64	123	20
128	144	24
256	169	28
512	189	31

b) Noise Shaping Technology

Noise shaping circuit is to extend the Dynamic range this result from the application of feedback. As we apply feedback this modulator acts as a closed loop modulator. A closed loop modulator can be used as a high pass filter for quantization noise and as a low pass filter for the input signal.

Noise shaping circuit is also used to reduce the bandwidth of selected signal. As we used Noise shaping technology the quantization noise is moved out of baseband so that SNR (Signal to

quantization noise Ratio) increases. As order of modulator increases noise shaping of the circuit becomes improve and SNR also increases.

Difference Amplifier:-

Difference Amplifier is a basic Block of Sigma Delta Modulator. 2 Inputs are applied to the Difference Amplifier. Out of these two inputs 1 is main input signal and another input is a output of DAC which is applied as a input to Difference amplifier. Circuit diagram and waveforms of Difference amplifier is as shown below.

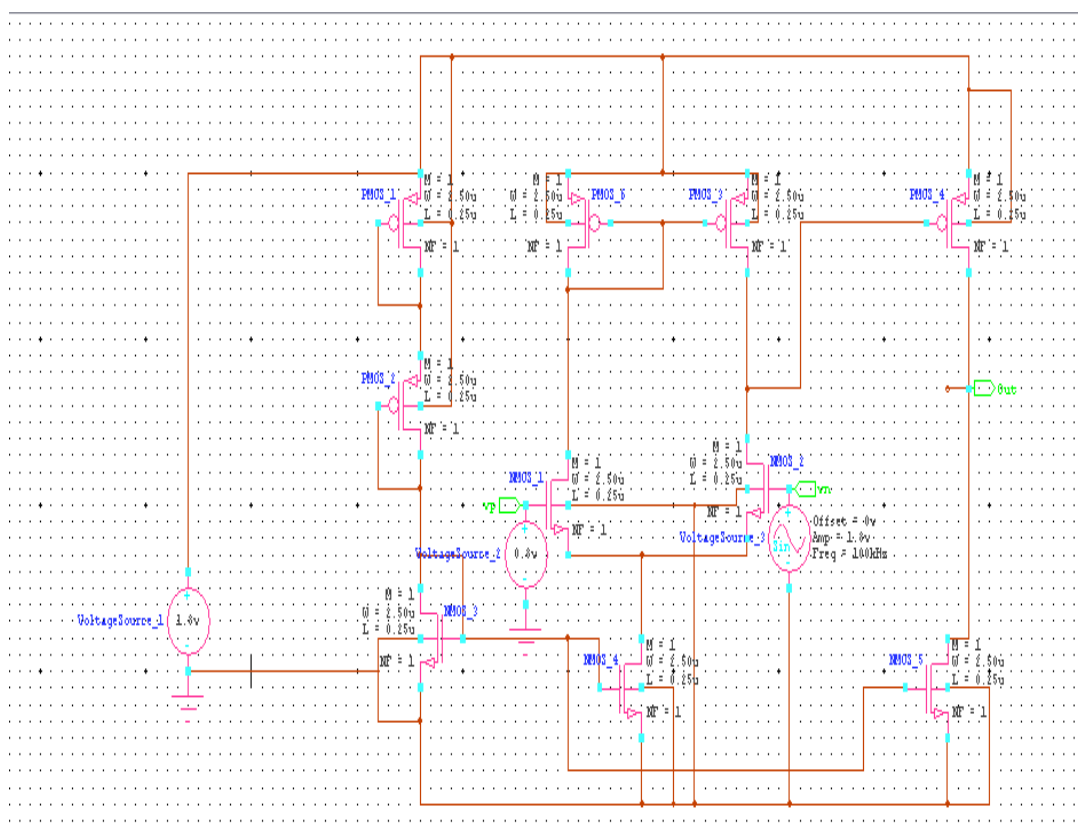


Figure 4: Structure of Difference amplifier

5. Integrator:-

An op-amp, a resistor, and a feedback capacitor comprise the integrator. The integrator's time constant is determined by the resistor and capacitor values. The time constant should be kept as little as possible. Otherwise, the integrator will enter saturation mode. The op-amp is at the heart of the sigma-delta modulator. It has a big open loop gain that allows the integrator to integrate smoothly while implementing the negative feedback principle. Furthermore, it has a broad enough bandwidth to pass at least the first two harmonics of the input sine wave. The developed op-amp has a big phase buffer in order to provide greater stability. Figure

4 depicts the implementation of an op-amp.

In the first order sigma-delta modulator, the 1-bit ADC is made up of a comparator and a DFF. The project employs a two-stage comparator to simplify the circuit. It is based on the previously mentioned two-stage op amp circuit. However, because stability is not an issue, the comparator does not need to be adjusted for close-loop feedback. This eliminates the need for an internal correction capacitor. As a result, the output slew rate increases. The schematic of the two-stage comparator is shown in Figure 5.

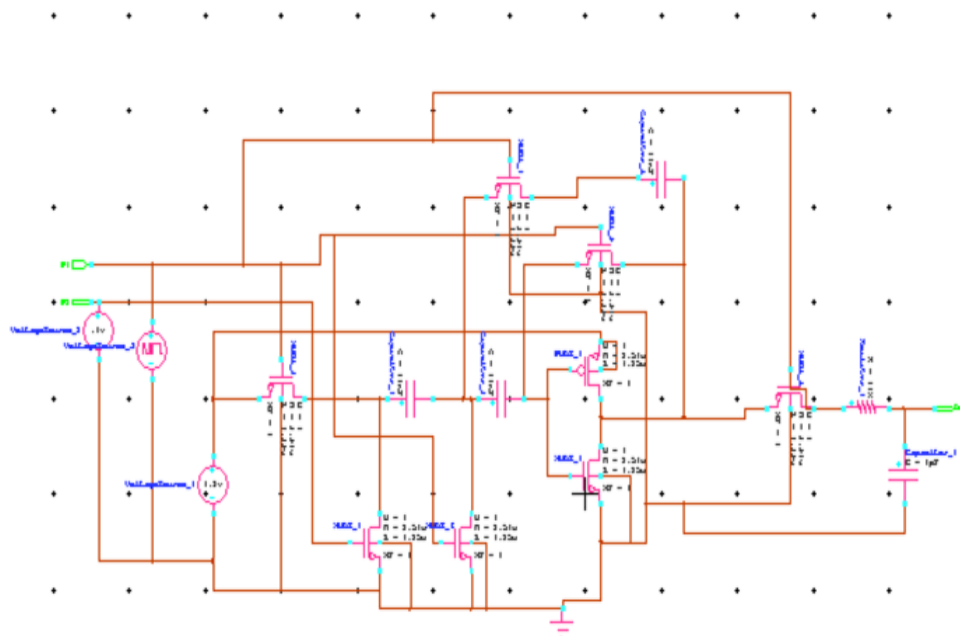


Figure 5: Structure of Op-Amp Based Integrator

1 bit ADC:-

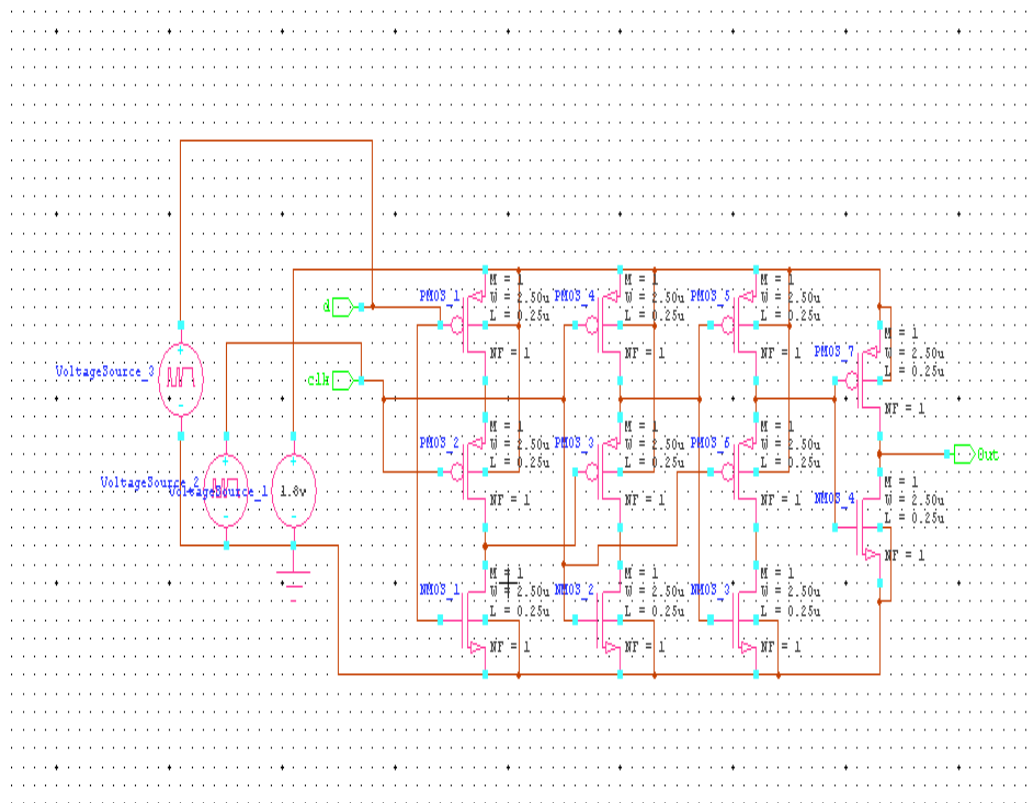


Figure 6:- Structure of 1 bit ADC

To supply steady current for the first stage differential inputs, N2 and N3 create a current mirror. P0, P1, N0, and N1 are differential amplifiers. The second stage is formed by P2 and N4 to magnify the signal from the first stage. Because the comparator in sigma-delta modulators must operate at a high oversampling frequency while having a resolution as little as 1 bit, the comparator design prioritises speed over accuracy.

The comparator's waveform is seen in the image below. Because the ADC output is

1 bit, a Decimator can be used to improve the resolution of the output. The equation

$$N = (50 \log k - 12.9) / 6.02$$

Where

N=Required Resolution

K=Over Sampling Ratio

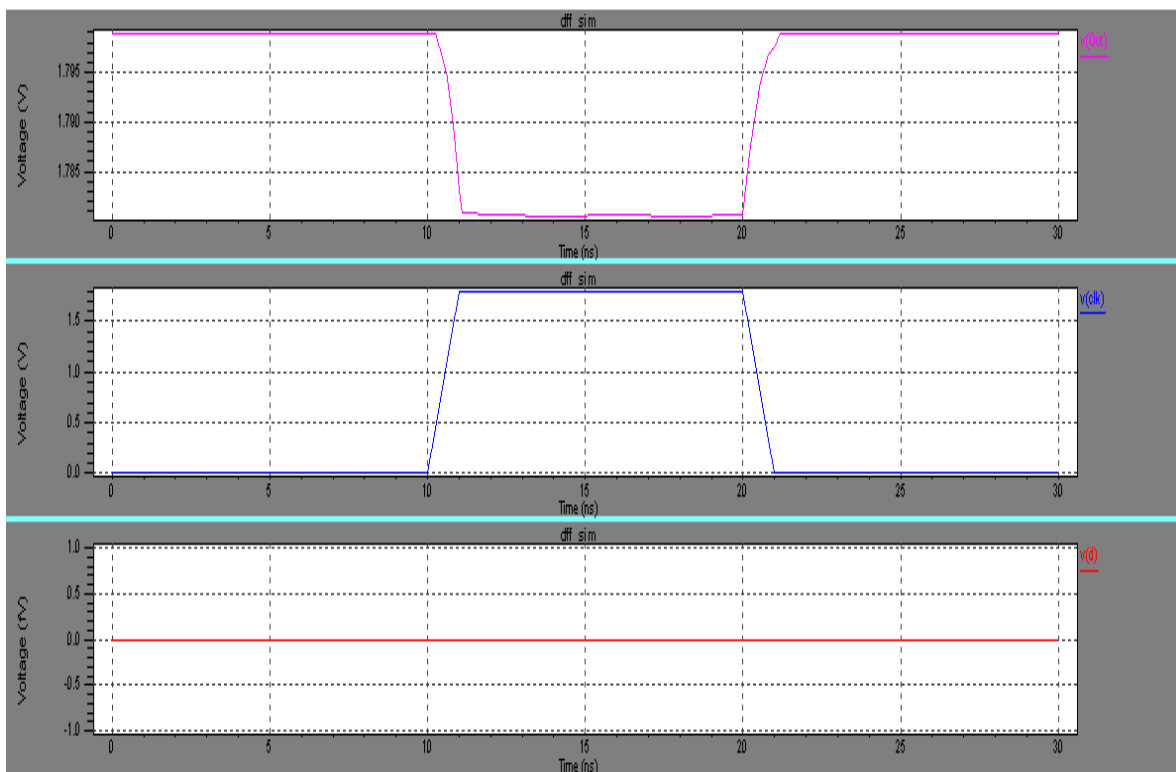


Figure 7: Output Waveform of 1 bit ADC

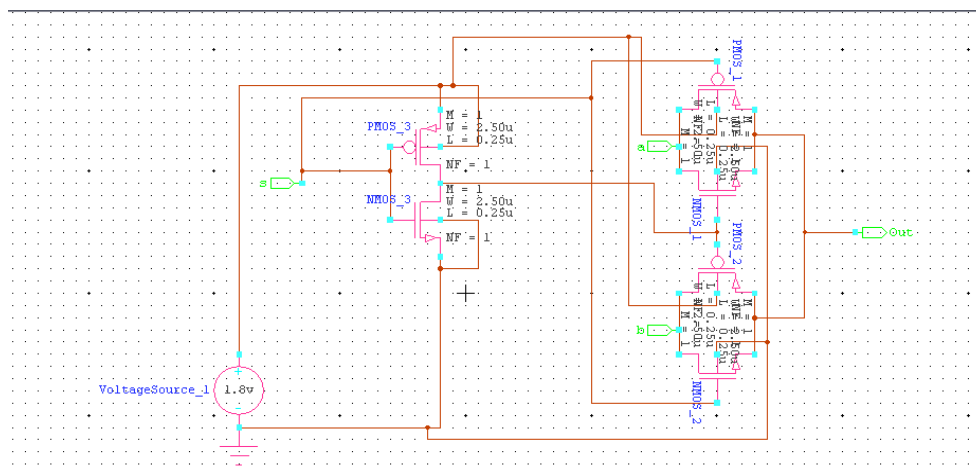


Figure 8: Structure of DAC

7. Digital to Analog Converter

A feedback DAC is used to transform a 1 bit binary representation into an analogue signal that will be provided as input to the Difference Amplifier through negative feedback, increasing the circuit's stability. Oversampling reduces the need for an anti-aliasing reconstruction filter. If a higher order filter is necessary to minimise the noise, some of the benefits of the sigma delta DAC design are lost.

8. Conclusion & Output Waveforms of Sigma Delta Modulator:-

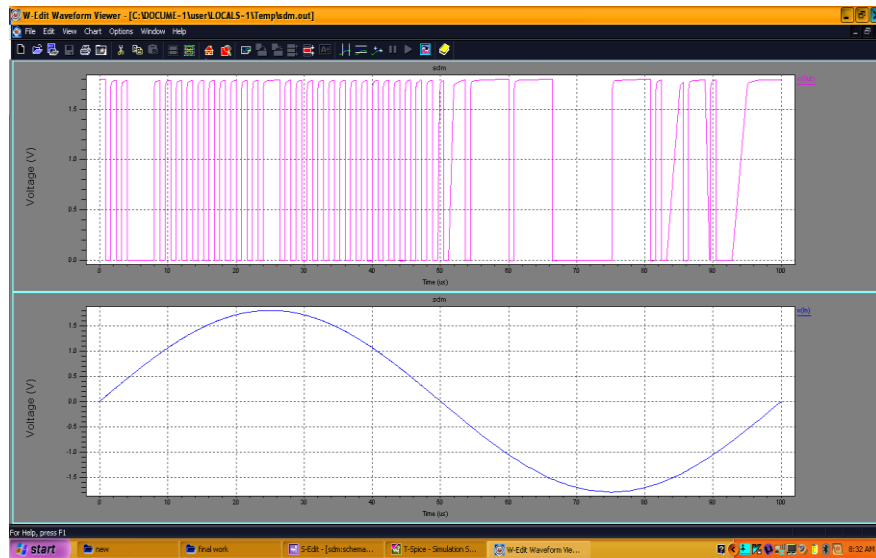


Figure 9:- Input output waveforms

REFERENCES

1. The Design of a High Speed and High Precision Sigma-Delta Modulator , Shuangwei Han and Yuliang Wang, Third International Conference on Information Science and Technolog March 23-25, 2013; Yangzhou, Jiangsu, China
2. Yves Geerts, Michiel Steyaert and Willy Sansen, “Design Of Multi-Bit Delta-Sigma A/D Converters”, Kluwer Academic Publishers, 2012.
3. R. Schreier and G. Temes, “Understanding Delta-Sigma Data Converters” ,IEEE press Piscataway, NJ, 2010.
4. T. V. Cao, D. T. Wisland, F. Moradi, and T. S. Lande, “Novel low voltage current-mirror sense amplifier based flip-flop with reduced delay time,” inCircuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on, pp. 3166–3169, IEEE, 2009.
5. T. V. Cao, D. T. Wisland, T. S. Lande, and F. Moradi, “Low phase-noise vco utilizing modified symmetric load and partial positive feedback for fdsm,” Analog Integrated Circuits and Signal Processing, Dec. 2011.
6. R. Wilcock, and M. Kraft, “Genetic algorithm for the design of electro-mechanical sigma delta modulator MEMS,” Sensors, 2011, vol.11, no.10, pp.9217-9232.
7. T. Northemann, M. Maurer, S. Rombach, A. Buhmann, and Y.

- Manoli, "A digital interface for gyroscopes controlling the primary and secondary mode using bandpass sigma-delta modulation," *Sensors and Actuators A: Physical*, August 2010, vol.162, no.2, pp. 388-393.
8. R. Schreier and G. Temes, "Understanding Delta-Sigma Data Converters", IEEE press Piscataway, NJ, 2005.
 9. U. Wismar, D. Wisland, and P. Andreani, "A 0.2 v 0.44/spl mu w 20khz analog to digital/spl sigma/delta modulator with 57 fj/conversion fom," in *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European*, pp. 187-190, IEEE, 2006.