

Design of Novel High Speed - Low-Power full adder cells using GDI Cell

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Abstract

With the rapid advances in VLSI Technology, design of digital circuits with high speed, low power consumption, high throughput and optimized area is a great challenge for an integrated circuit designer. In Digital design adders are key components, where they perform various functions like addition, subtraction, multiplication and division. Multi-bit width adders are required in Very Large-Scale Integrated circuits (VLSI) for processing of microcontrollers, microprocessors, data processing, Application Specific Integrated Circuits (ASICs) and Digital signal processors. In this Paper various adder cells such as CCMOS, CPL, Hybrid Adder, GDI and proposed GDI full adder cells are analyzed and compared with respect to Delay, Power Dissipation, Power Delay Product and Area. The Gate Diffusion Input (GDI) technique has been used for generation of digital logic functions. This technique is compared with other full adder techniques which allow less power consumption and reduced propagation delay with minimum number of transistors. The speed of the circuit is limited by size of the transistors, parasitic capacitance and delay. An important parameter that evaluates circuit performance is Power Delay Product (PDP) which depends on power consumption and speed. Simulations are performed by Mentor graphics 130nm CMOS technology ELDO simulator. Performance is compared by varying power supply voltages. The analysis has been done on the basis of propagation delay, power consumption and power delay product. Reduction in power-delay product is achieved by the proposed GDI technique.

Keywords: Gate Diffusion Input (GDI), Low Power Design, complex logic, Power characteristic, Analysis, CMOS, delay, digital, Power Delay Product, performance, VLSI.

I. INTRODUCTION

Arithmetic operation is exclusively used for in most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors. The most frequently use operation for the MAC units are Addition, subtraction, multiplication, and multiply and accumulate (MAC). For any such applications, 1-bit full-adder cell is the basic building block. The design complexity of a digital circuits is mainly depend on number of transistors, area, topology selection, power dissipation and speed for high speed, low power application and better performance.

A better metric would be the power delay product or energy consumption per operation to indicate the optimal design tradeoffs. At low supply voltage, performance of the CMOS circuit is degraded. But my scaling down the threshold voltage performance losses can be limited to some extent which results in high leakage current [2-4].

For low power design, Clock gating technique and dynamic voltage/frequency scaling techniques are used.[4-6]. The supply voltage is scaled down below threshold voltage by sub-threshold circuit design, the charged/discharged sub-threshold leakage currents are made through load capacitances.

The total power dissipated in generic digital CMOS gate is calculated by Equation (1 - 4)

$$P_{total} = P_{dynamic} + P_{shortcircuit} + P_{static} \quad (1)$$

$$P_{dynamic} = P.C_L.f.V_{DD}^2 \quad (2)$$

$$P_{shortcircuit} = I_{peak}.t_{SC}.V_{DD}.f \quad (3)$$

$$P_{static} = I_{static}.V_{DD} \quad (4)$$

Where

P = Change state probability of gate.

F = frequency

CL = Load Capacitance

VDD = Supply Voltage

I_{peak} = Maximum current during the status of gate

t_{SC} = sort circuit time

I_{static} = static current

There are three major components of power dissipation in complementary metal–oxide–semiconductor (CMOS) circuits.

- 1) Switching Power,
- 2) Short Circuit Power,
- 3) Static Power.

Dynamic power constitutes the majority of the power dissipated in CMOS VLSI circuits. It is the power dissipated during charging or discharging the load capacitances of a given circuit [2]. Power consumption of the circuit is reduced by reducing any of the component parameters. It is of equal importance to increase the system-clock frequency for faster operation.

A Full Adder is a three-input two-output block, where the inputs are the two bits to be summed, A and B, and the carry input bit, C_{in} , which derives from the calculations of the previous digits. The outputs are the result of the sum operation, S, and the resulting value of the carry output bit, c_{out} . More specifically, the sum and carry output are given by

$$S = A \oplus B \oplus C_{in} = \overline{\overline{A}\overline{B}C_{in}} + \overline{\overline{A}B\overline{C_{in}}} + \overline{\overline{A}B\overline{C_{in}}} + \overline{ABC_{in}} - 1$$

$$C_{out} = \overline{C_{in}}(AB) + C_{in}(A + B) - 2$$

Power consumption is the lowest supply voltage in which the design can still operate properly. Various full adder designs techniques are available in the literature [7–14] which they have their own merits and demerits. Some of which are as follows Static CMOS, dynamic circuit, transmission gate, or pass transistor logic. The conventional full adder design is a static CMOS with complementary pull-up pMOS and pull-down nMOS networks, which requires 28 transistors and provides full-swing output and good driving capabilities [9,11].

Complementary pass-transistor logic (CPL)[9] provides high-speed, full-swing and good driving capability due to the output static inverters and the fast differential stage of cross-coupled pMOS transistors. Other full-adder designs like transmission-function full adder (TFA) [10] and transmission-gate full adder (TGA) [11].

An adder cell designed and implemented with more than one logic style is called as

hybrid CMOS logic design style. Examples of adders built with this design style are DB cell [12], NEW14-T adder [13], and hybrid

pass logic with static CMOS output drive full adder [14] and new-HPSC [15] adder, ULPFA adder design [17].

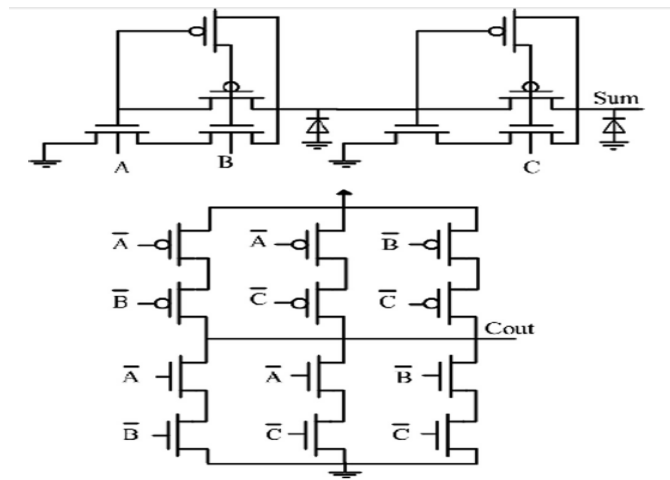


Figure 1: Ultra Low-power Full adder design

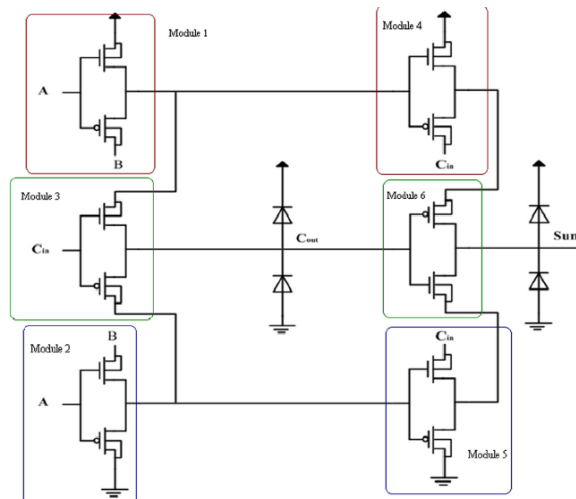


Figure 2: GDI- MUX full adder design.

Pass transistor logic (PTL) can be used to design an adder with lower number of transistor than that of transmission gate adder. In pass transistor logic, XOR/XNOR operation can be obtained by using 4 transistors only, but output voltage level is degraded at certain input combinations [18].

To overcome the problem that occurs in the previous techniques like PTL, CPL, Transmission gate, DPL etc., Gate diffusion input (GDI) technique is implemented for low-power and high efficient design technique[19]. It is a genius, fast and power design with lesser number of transistor counts, while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

II. THE GDI TECHNIQUE

a) GDI Cell

The GDI method which is first proposed by A. Morgenshtein, A. Fish, and I. A. Wagner in 2001[19], GDI method is based on the use of a simple cell as shown in Figure 2 [19,20]. The basic GDI cell reminds as a standard CMOS inverter but have important differences that are to be considered:

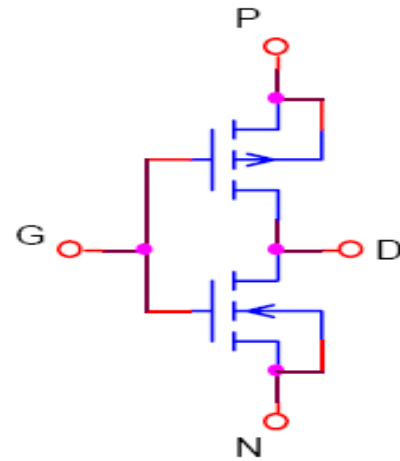


Figure 3: Basic GDI Cell Unit

- 1) GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
- 2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies.

TABLE I: Some Logic Functions That Can Be Implemented With a Single Gdi Cell [19].

N	P	G	Output	Function
'0'	B	A	$\overline{AB}$	F1
B	'1'	A	$\overline{A} + B$	F2
'1'	B	A	$A + B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{AB} + AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

By using a basic Gate Diffusion Input (GDI) cell multiple Boolean functions can be implemented. Functional design of GDI cell is the extension of a single input CMOS inverter structure into a triple input GDI cell. Different Boolean functions (Table 1) can be achieved by changing the input configuration of the GDI cell.

In Static CMOS circuit implementation these functions needs relatively complex (6–12 transistors) but it is very efficient with the GDI cells. The complex function like multiplexer can be implemented by only two transistor GDI cell.

The output functions of basic GDI cell are based on Shannon expansion. Output

expressed in term input P, N and G as follows.

$$Out = G'P + GN \quad - 3$$

The main drawback of the GDI technique is it suffers from threshold voltage drops which reduce current drive and therefore affect the performance of the gate and increase static power dissipation in the cascaded inverters, used for swing restoration.

But this is not a good quality solution because adding buffer after every logic cell will lead to increased area and reduced delay. By using multiple Threshold transistors (Multi VTH) in swing restoration buffer the power dissipation can be reduced [20,21].

b) GDI-MUX full adder

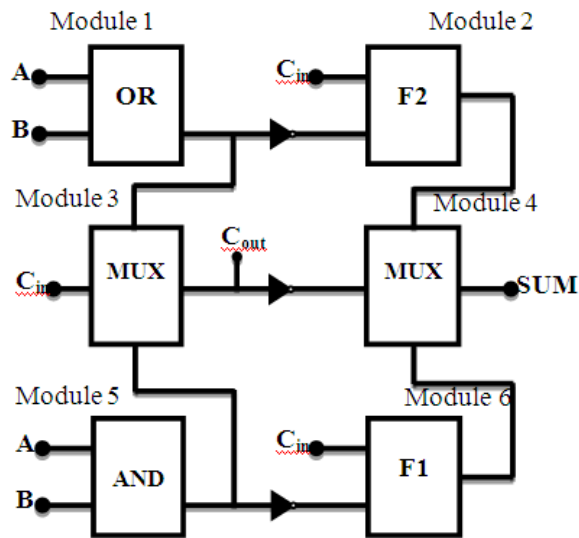


Figure 4: Proposed GDI-Based full adder block diagram.

A new design approach for a full adder cell is implemented in this paper by eliminating complicated XOR- XNOR logic. From the full adder Truth-Table it can be seen that C_{out} is equal to $(A \text{ AND } B)$ when $C_{in} = '0'$, and C_{out} is equal to $(A \text{ OR } B)$ when $C_{in} = '1'$. Thus, output C_{out} can be obtained by multiplexing when $C_{in} = '0'$ and $C_{in} = '1'$. The same criteria is applicable for output SUM, when $C_{out} = '0'$, the SUM output is equal to $(A \text{ OR } B \text{ OR } C_{in})$, and when $C_{out} = '1'$, the SUM is $(A \text{ AND } B \text{ AND } C_{in})$. Now C_{out} can be used to selection line for multiplexer when $C_{out} = '0'$ or $'1'$. Hence, an alternative logic scheme to design a full adder cell can be formed by AND, OR and

MUX logic blocks as shown in Fig.2 [1]. But in order to obtain full voltage swing at the output, design of the adder cell is modified by placing an three HVT inverter (6 Transistors) and functional blocks instead of four ultra-low power diodes (8 transistors) in [1]. A GDI technique is used for this full adder implementation. Silicon on Insulator (SOI) process is required for implementation of Gate Diffusion Input (GDI) scheme.

The Block diagram GDI-Based full adder is shown in Fig. 4. In order to implement $(A \text{ OR } B)$, N input is connected to V_{DD} , P input is connected to B and G is connected to A of

a GDI Cell (Module.1). For the Logic AND operation ($A \text{ AND } B$) is implemented by connecting P terminal to ground, N is connected to input B and G is connected to input A (Module 5) in figure 4. For the output C_{out} GDI cell is used as multiplexer as in module 3, where output of module 1 ($A \text{ OR } B$) is connected to the N terminal of the cell, output of module 5 ($A \text{ AND } B$) is connected to P terminal of the cell and selection line C_{in} is connected to G terminal.

Output of module 2 should be ($A \text{ OR } B \text{ OR } C_{in}$) can be obtained by inverting the output of module 1 using HVT buffer and function $F2 = \overline{A+B}$ is implemented by connecting P terminal to V_{DD} , N terminal to C_{in} and G is connected to inverted output of module 1. Similarly Output of module 6 ($A \text{ AND } B \text{ AND } C_{in}$) which is obtained by inverting the output of module 5 using HVT buffer and function $F1 = \overline{A \cdot B}$ is implemented by connecting N terminal to Ground, P terminals to input B and G to inverted output of module 5.

Finally in order to produce the SUM, GDI is used as a multiplexer with its G input

connected to C_{out} and finally its P and N inputs are linked to ($A \text{ OR } B \text{ OR } C_{in}$) and ($A \text{ AND } B \text{ AND } C_{in}$) respectively.

c) 8T GDI Full adder

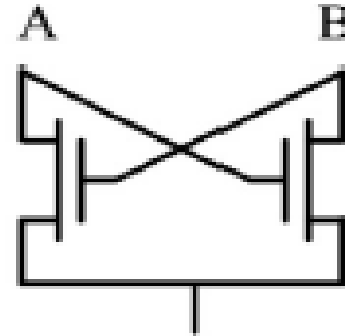


Figure 5 : SEMI XNOR Gate.

A novel Low-Power 8T GDI full adder have been proposed with an enhanced speed and low power characteristic is proposed. SEMI XOR-XNOR gates[26] have been employed and its truth table is as shown in Table II.

The circuit demonstrated in figure.5 is flexible, robust and Low-Power XNOR Logic gate circuit. Semi XNOR logic gate output is obtained with inputs say 'B' and 'C' as $B \odot C$ and this output of the XNOR gate (N2) is connected to the GDI inverter to get XOR logic (N1).

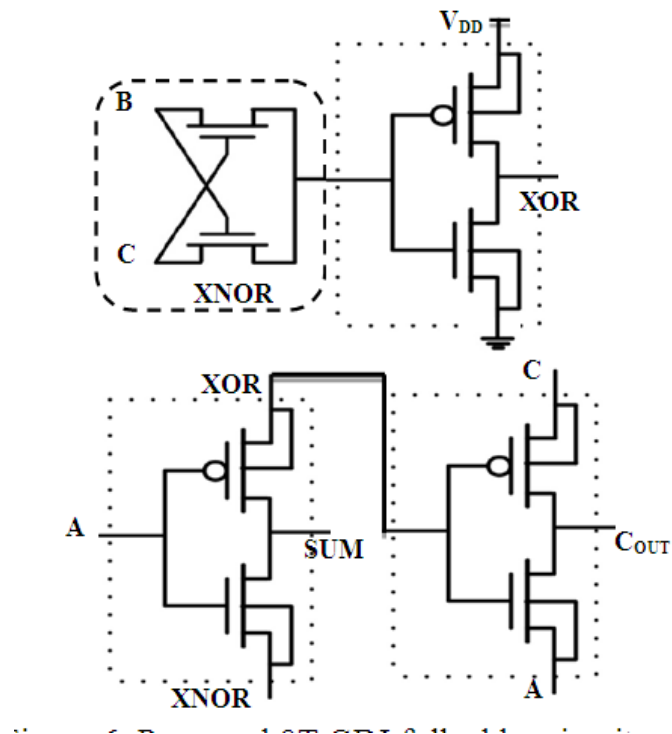


Figure 6: Proposed 8T GDI full adder circuit.

TABLE II: TRUTH TABLE FOR SUM AND C_{OUT}

A	B	C _{in}	Sum	C _{out}	Semi -XOR	Semi-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

The output of these two logics ‘XNOR’ and ‘XOR’ gate as the two inputs for the multiplexer with input ‘A’ as selection in GDI cell. The output SUM obtained as

$$SUM = \bar{A} \cdot N1 + A \cdot N2$$

-4

Similarly output C_{OUT} can be obtained by using the GDI cell as a multiplexer with two inputs ‘A’ and ‘C’ with a selection input as $N1 = (B \oplus C)$ then C_{OUT} is

$$C_{OUT} = \bar{N1} \cdot C + N1 \cdot A = \overline{(B \oplus C)} \cdot C + (B \oplus C) \cdot A$$

-5

A new full adder cell have been proposed in this paper as shown in figure 7. This adder cell is evaluated and compared to other full adder cell from the literature. Implementation of various types of full adder cell are implemented using Mentor graphics schematic and layout editor and extracted using 130nm CMOS technology. Simulations are carried out using ELDO, with the capacitances and resistances extracted from the layout. These full adder cells are simulated with 100 MHz frequency and at 27°C and the supply voltages varying from 0.8 to 1.4V.

SIMULATION RESULTS AND ANALYSIS

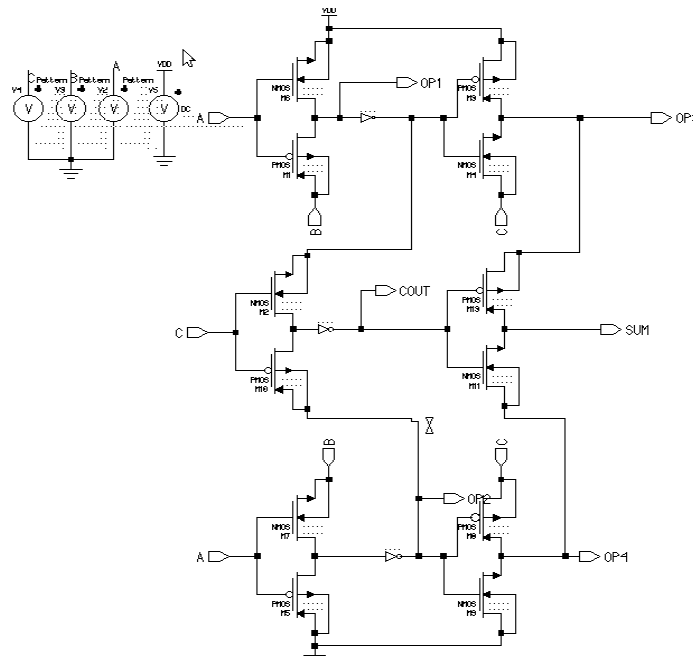


Figure 7: Test for Proposed GDI-Based full adder circuit.

The threshold voltages of the pMOS and nMOS transistors are around 0.34 V. As Full adder cells are basic building block for any arithmetic circuit which need to be cascaded to perform an arithmetic operation. But performance of the full adder cell is degraded dramatically or cell becomes non-operative at low supply voltage due to its lack of driving power capability that results as a failure in simulation. Therefore, the full adder cells must possess sufficient

drivability to provide the next cell with clean inputs [24].

For practical applications, a 16 full adder cells are cascaded using proposed full adder cell. This 16 bit cascaded structure simulates the circuit like binary adders and multipliers. Buffers are used at the inputs to get proper loading conditions and more realistic input signals.

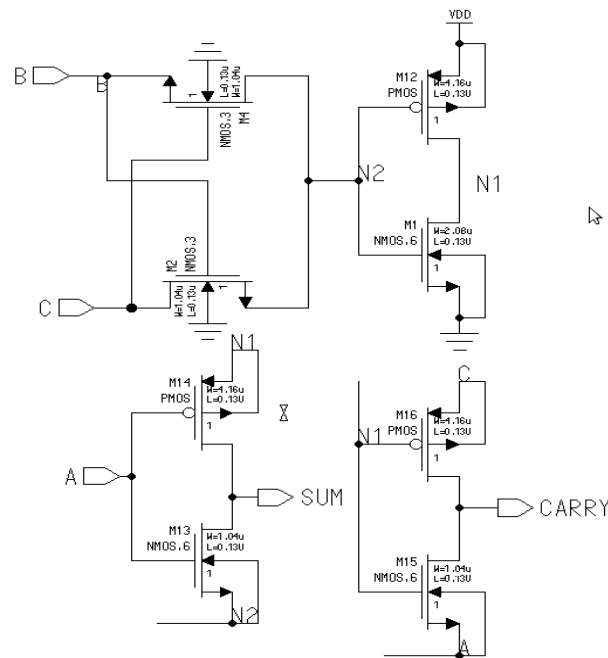


Figure 8 : Test for Proposed 8T GDI full adder circuit.

For an accurate result, all the required input pattern- to-input-pattern transitions are included in the test patterns. Propagation delay, Power dissipation and power delay

product are measured for the whole 16 bit adder. Comparison of full adder cells are on the basis of Power, Delay, PDP and Area.

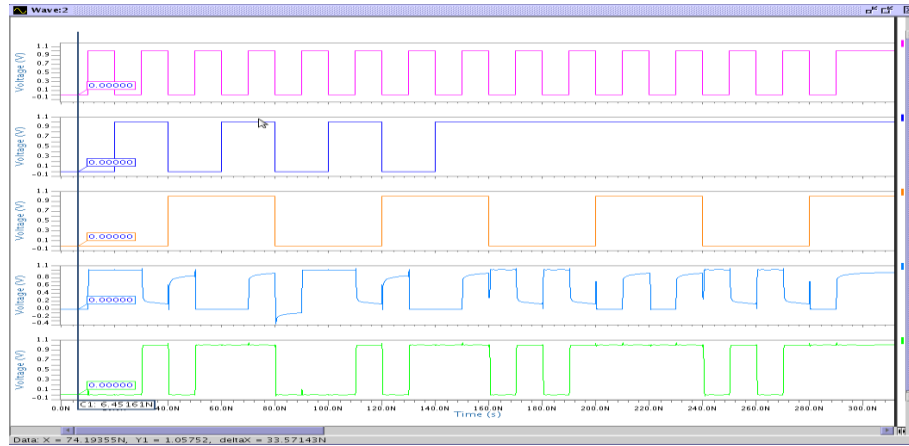


Figure 9: Input/output waveform of Proposed GDI based Full adder circuit

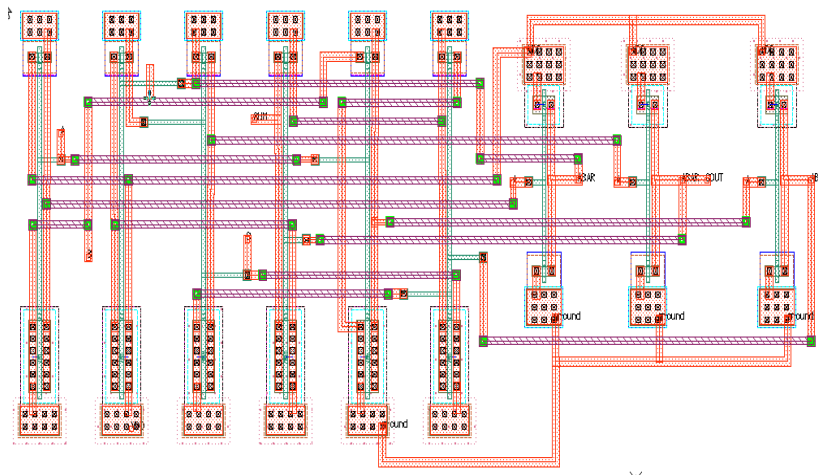


Figure 10: Layout for Proposed GDI Full adder circuit

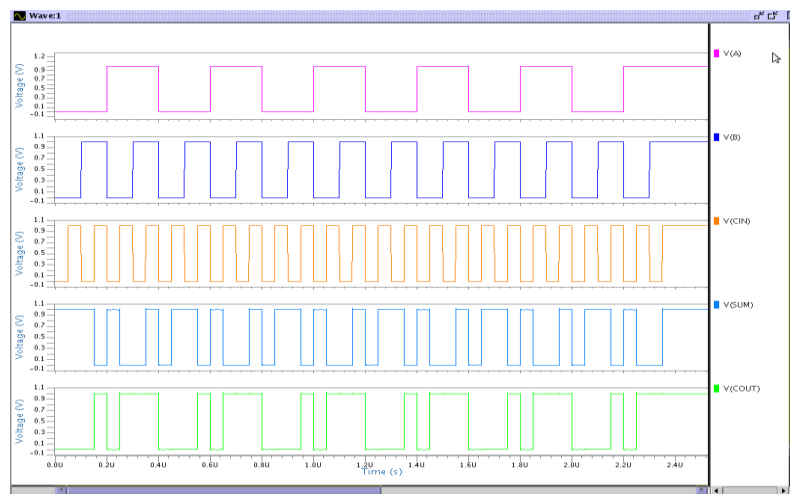


Figure 11: Input/output waveform of Proposed 8T GDI Full adder

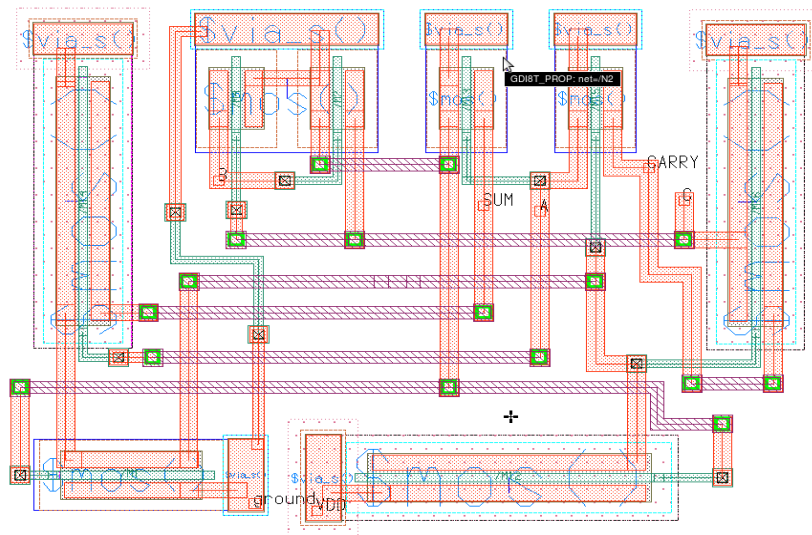


Figure 12: Layout for Proposed 8T GDI Full adder

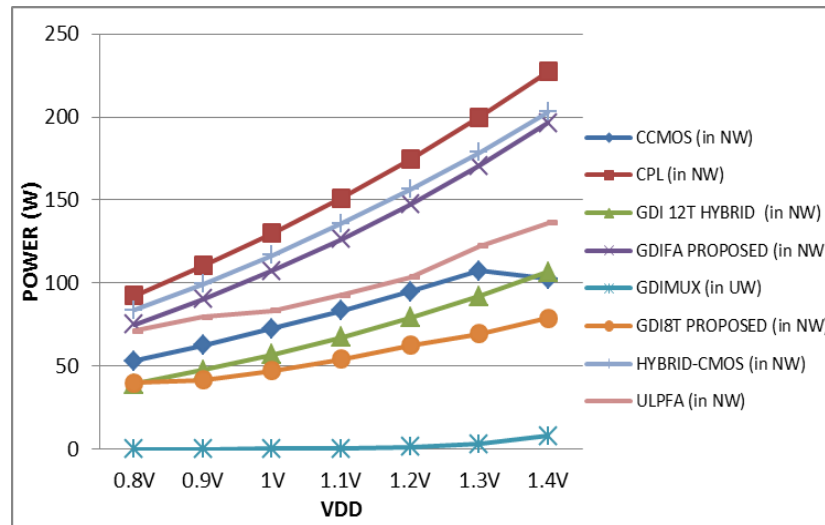


Figure 13: Power results for different supply voltages in 130nm

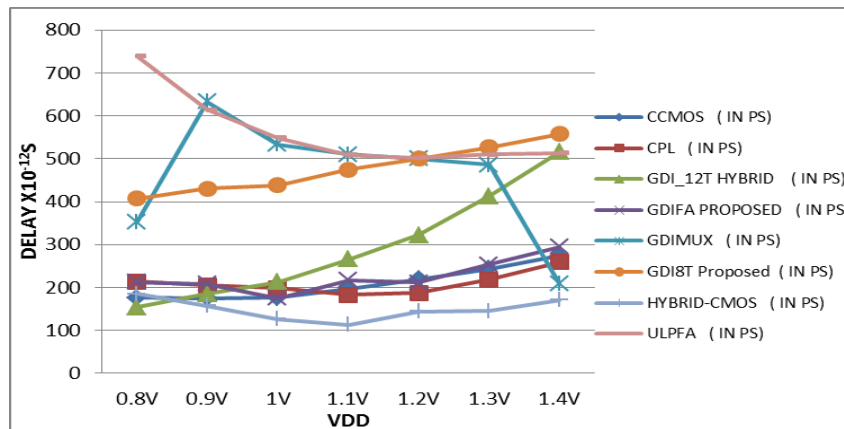


Figure 14: Delay results for different supply voltages in 130nm

The Power Delay product (PDP) is a quantitative measure of the efficiency and a compromise between power dissipation and speed. Whenever low power applications are required Power Delay Product is important factor to be considered. The power

dissipation, delay and Power delay Product for C-CMOS, CPL, Hybrid full adder, ULPFA and other GDI based adder cells are evaluated and determined under different supply voltages (0.8–1.4 V).

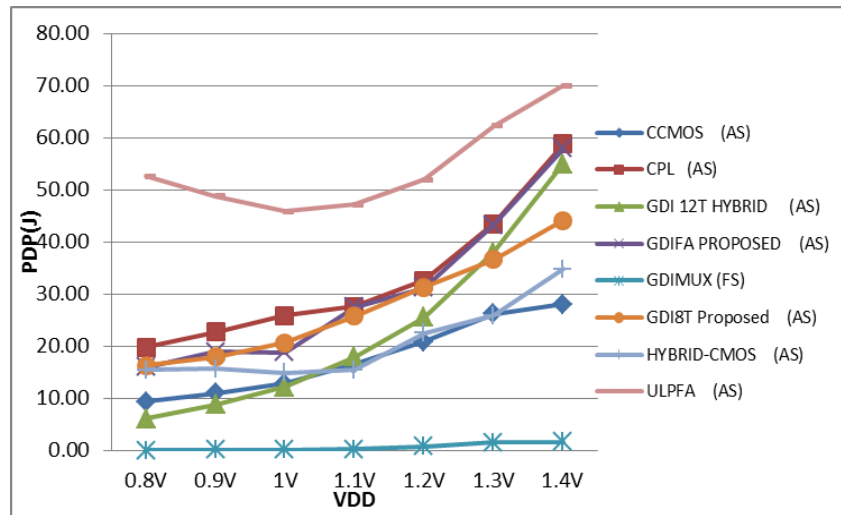


Figure 15: PDP results for different supply voltages in 130nm

TABLE III: Simulation Results For Full Adders in 130nm With $F=100$ Mhz And 1.2v VDD

Adder Technique	power ($\times 10^{-9}$ W)	Delay ($\times 10^{-12}$ S)	PDP ($\times 10^{-18}$ J)	Device Count
CCMOS	94.99	219.3	20.83	28
CPL	174.556	186.86	32.62	32
GDI HYBRID	79.123	322.19	25.49	20
GDI FA PROPOSED	147.5	211.06	31.13	18
GDIMUX	1.49015	500.09	0.75	20
8T GDI PROPOSED	62.42	500.3	31.23	8
HYBRID-CMOS	156.42	143.63	22.47	24
ULPFA	103.52	502.09	51.98	24

Table III shows the power consumption, propagation delay and Power Delay Product (PDP) values for 1.2V for 130nm CMOS technology and 16 bit full adder circuit is considered. Delay is calculated from 50% of the input signal voltage to 50% of the output signal voltage. It can be observed that two Proposed GDI based Full adder cells has the smallest delay and thus faster than C-CMOS, CPL, Hybrid full adder, and ULPFA full adders.

Figures 13 to 15 shows the power consumption, propagation delay and Power Delay Product (PDP) of the 16 bits ripple carry adder. Complementary pass transistor Logic Full adder cell consumes more power due to its dual-rail structure, large number of internal nodes and static inverter utilization which are the main source of leakage and static power dissipation.

The proposed GDI based full adder cell and proposed 8T GDI full adder has lower power dissipation and lower switching capacitance. Among these various full adder cells, the proposed two GDI based full adder has best performance, High speed, Low power and improved logic level swing. It has been observed that proposed GDI based full adder uses only 18 transistors and proposed 8T GDI uses only 8 transistors.

The GDI-based full adder has the best PDP in comparison with its counterpart and have the smallest area because of less number of transistors and its optimized and symmetric arrangement.

CONCLUSIONS

In this paper a two novel full adder cells using GDI (Gate-Diffusion Input) cell for Low-Power and high speed application is proposed. This designed full adder cell successfully operates at low voltages with high driving capability and excellent signal integrity. Using 130nm CMOS technology an optimized GDI-Based full adder cell is studied for energy efficiency and high speed. Simulations have been carried out using Mentor Graphics ELDO simulator to evaluate the new design and also other adder cell, including C-CMOS, CPL, Hybrid full adder, ULPFA.

A wide comparison made for the designs described in the literature and a significant improvement in terms of Delay, power dissipation and Power-Delay product (PDP) parameter are illustrated. A large area reduction and reduction on switching activity is achieved significantly reducing the number of transistors used in the circuit. This considerable reduction in power by

minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

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