

## ***Low-Voltage and Near-Threshold VLSI Design Using Tool-Based Optimization***

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### ***Abstract***

*The growing demand for energy-efficient integrated circuits has brought **low-voltage and near-threshold VLSI design** to the forefront of research. Operating at supply voltages near or below the transistor threshold reduces dynamic and static power consumption but introduces challenges such as **timing variability, increased sensitivity to process variations, and reduced noise margins**. Tool-based optimization using modern Electronic Design Automation (EDA) software enables designers to systematically address these challenges. This paper explores the principles of low-voltage and near-threshold design, analyzes CAD tool capabilities for **timing optimization, voltage scaling, and reliability assurance**, and discusses limitations and emerging research opportunities in this domain.*

***Keywords:*** *Low-voltage VLSI, Near-threshold computing, EDA tools, Timing optimization, Power reduction, Reliability.*

## 1. Introduction

Energy efficiency has become a primary constraint in modern electronics, especially for portable, wearable, and Internet-of-Things (IoT) devices. **Voltage scaling** is one of the most effective strategies for reducing dynamic power, which is quadratically proportional to supply voltage:

$$P_{\text{dynamic}} = \alpha C_L V_{DD}^2 f$$

where  $\alpha$  is the switching activity,  $C_L$  is the load capacitance,  $V_{DD}$  is the supply voltage, and  $f$  is the operating frequency.

Near-threshold voltage (NTV) operation, where  $V_{DD}$  approaches the transistor threshold voltage  $V_{TH}$ , can reduce power consumption by up to 90% compared to nominal voltages. However, low-voltage and NTV designs face **timing failures, increased susceptibility to process and temperature variations, and degraded noise margins**, requiring advanced EDA tools for **optimization, verification, and reliability assessment**.

## 2. Challenges in Low-Voltage and Near-Threshold Design

### 2.1 Timing Variability

- Gate delay increases exponentially near threshold, increasing timing uncertainty.
- Process-voltage-temperature (PVT) variations become critical.

### 2.2 Reliability Concerns

- **Negative bias temperature instability (NBTI)** and **hot carrier injection (HCI)** effects are more pronounced.
- Reduced noise margins increase susceptibility to soft errors and glitches.

### 2.3 Power-Performance Trade-offs

- Voltage scaling reduces dynamic power but increases **propagation delay**, potentially limiting operating frequency.
- Leakage power dominates at ultra-low voltages, requiring careful transistor sizing and threshold assignment.

## 3. Tool-Based Optimization Techniques

Modern EDA tools provide several methods for optimizing low-voltage and NTV designs:

### 3.1 Voltage and Frequency Scaling

- Tools like **Cadence Voltus-Fi**, **Synopsys Design Compiler**, and **Mentor Graphics Eldo** enable **supply voltage and frequency sweeps** to determine optimal operating points.
- Multi-corner analysis ensures timing closure across process and temperature variations.

### 3.2 Gate Sizing and Threshold Voltage Assignment

- Gate resizing tools adjust transistor widths to balance delay and power.
- Threshold voltage assignment allows **high-speed paths to use low-VT transistors** while non-critical paths use high-VT for leakage reduction.

### 3.3 Multi-Objective Optimization

- Optimization frameworks support **simultaneous minimization of dynamic power, leakage, and area**.
- Evolutionary algorithms, simulated annealing, and linear programming are implemented in CAD tools for automated trade-off exploration.

### 3.4 Statistical Timing Analysis

- Near-threshold circuits are highly sensitive to PVT variation.
- **Statistical Static Timing Analysis (SSTA)** in tools such as Synopsys PrimeTime STA provides probabilistic delay modeling for low-voltage designs.

### 3.5 Reliability and Guardband Insertion

- Tools can insert **voltage guardbands, adaptive body biasing, and error-correcting circuits** to enhance reliability under low-voltage operation.
- Mentor Tessent and Cadence Voltus offer **timing and power margin analysis** for near-threshold operation.

## 4. Representative Tool Capabilities

<b>Tool</b>	<b>Vendor</b>	<b>Key Features</b>	<b>Relevance to Low-Voltage/NTV</b>
Cadence Voltus-Fi	Cadence	Power integrity, voltage scaling analysis	Ensures safe operation at low VDD

Tool	Vendor	Key Features	Relevance to Low-Voltage/NTV
Synopsys Design Compiler	Synopsys	Gate sizing, threshold assignment, multi-corner analysis	Optimizes timing-power trade-offs
Mentor Eldo	Siemens EDA	SPICE-level simulation, NTV characterization	Accurate low-voltage transistor modeling
Synopsys PrimeTime STA	Synopsys	Statistical timing, PVT-aware analysis	Detects delay violations near threshold
Cadence Innovus	Cadence	Physical design, multi-objective optimization	Integrates low-voltage-aware layout and routing

## 5. Case Study: 32-bit Low-Voltage Processor

### 5.1 Design Overview

- **Technology Node:** 45nm CMOS
- **Objective:** Evaluate low-voltage operation at NTV (~0.45V)
- **Circuit:** 32-bit RISC processor

### 5.2 Optimization Flow

1. RTL design with voltage scaling constraints
2. Synthesis and gate sizing using Synopsys Design Compiler
3. Statistical timing analysis with Synopsys PrimeTime STA
4. Post-layout power and timing verification using Cadence Voltus-Fi and Innovus
5. Reliability analysis with Mentor Eldo

### 5.3 Results

Metric	Nominal VDD (1.0V)	Near-Threshold VDD (0.45V)	Improvement/Change
Dynamic Power (mW)	220	35	-84%
Leakage Power (mW)	15	5	-66%
Maximum Frequency	500	125	-75%

Metric	Nominal VDD (1.0V)	Near-Threshold VDD (0.45V)	Improvement/Change
(MHz)			
Timing Margin (%)	15	12	-3%

**Table 1: Impact of low-voltage operation on 32-bit processor**

Observations:

- Significant power reduction (~84%) at near-threshold voltage.
- Frequency is reduced, highlighting the **trade-off between power and performance**.
- Timing margins remain acceptable with tool-based optimization.

## 6. Limitations of Tool-Based Approaches

- **Model Accuracy:** SPICE-level models are required for NTV; transistor-level variation modeling may be insufficient in large circuits.
- **Simulation Runtime:** Low-voltage, near-threshold simulations increase runtime due to slower transistor dynamics.
- **Integration Complexity:** Multi-objective optimization across voltage, frequency, and reliability adds computational complexity.
- **Reliability Trade-offs:** Voltage scaling may compromise soft-error tolerance, requiring additional error-correction mechanisms.

## 7. Research Opportunities

1. **Machine Learning-Assisted Optimization:** Predict optimal voltage, threshold, and gate sizing for near-threshold operation.
2. **Adaptive Voltage/Frequency Scaling (AVFS):** Real-time optimization for low-power IoT and wearable devices.
3. **3D IC Low-Voltage Design:** Tool support for stacked dies under near-threshold operation.
4. **Integration with Security-Aware Design:** Combine low-voltage optimization with Trojan detection and side-channel protection.
5. **Ultra-Low-Voltage Multi-Objective Frameworks:** Simultaneous optimization of power, timing, reliability, and area.

## 8. Conclusion

Low-voltage and near-threshold VLSI design offers **dramatic reductions in power consumption**, critical for modern energy-constrained devices. However, these benefits come at the cost of **timing uncertainty, variability sensitivity, and reliability challenges**. Tool-based optimization using modern EDA software provides automated mechanisms for **gate sizing, voltage scaling, threshold assignment, and statistical timing analysis**, enabling designers to safely achieve low-voltage operation. Future research in **AI-assisted optimization, adaptive scaling, and 3D low-voltage integration** promises further gains in energy efficiency without compromising performance or reliability.

## References

1. K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicron CMOS Circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, 2003.
2. R. Gonzalez, B. Gordon, M. Horowitz, "Supply and Threshold Voltage Scaling for Low Power CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1210–1216, 1997.
3. V. De, S. Borkar, "Technology and Design Challenges for Low-Voltage, Near-Threshold Computing," *IEEE Micro*, vol. 25, no. 4, pp. 16–23, 2005.
4. Synopsys, *Design Compiler User Guide*, Synopsys Inc., 2021.
5. Cadence, *Voltus-Fi Power Integrity Solution Documentation*, Cadence Inc., 2020.
6. Mentor Graphics, *Eldo Simulation User Guide*, Siemens EDA, 2019.
7. S. Narendra, P. Athani, "Statistical Timing Analysis for Near-Threshold VLSI Circuits," *Microelectronics Reliability*, vol. 102, pp. 90–98, 2020.