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A Survey on Register Transfer Logic Fault Modeling (RTL)

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Abstract

This research aims to testing of digital circuits. By using fault models at the lower levels, testing becomes cumbersome and will lead to delays in the design cycle. Thus there is a need to look for a new approach of testing the circuits at higher levels to speed up the design cycle. Different methods are implemented to detect the faults such as stuck-at faults in RTL circuits. A digital circuit usually comprises a controller and data path.

The time spent for determining a valid controller behavior to detect a fault usually dominates test generation time. A validation test set is used to verify controller behavior and, hence, it activates various controller behaviors. In this paper, different methods are presented for detecting faults in the data path thus, resulting in the detection of a majority of stuck-at faults in the data path RTL modules

.

Keywords: *stuck-at faults; fault coverage; data structure; validation test sets*

INTRODUCTION

There are following faults in the chip namely Single stuck-at faults; Transistor open and short faults; Memory faults; PLA faults (stuck-at, cross- point, bridging); Functional faults (processors); Delay faults (transition, path); Analog faults.

Three properties define a single stuck-at fault:

1. Only one line is faulty

2. The faulty line is permanently set to 0 or 1

3. The fault can be at an input or output of a gate.

Advances in semiconductor and electronic design automation technology have increased the size and complexity of VLSI circuits.Various invasive [design for testability (DFT)] and noninvasive [software-based self-test (SBST), built-in self-test (BIST)] strategies have been suggested to reduce test generation time and improve fault coverage. While the invasive techniques tend to alter the characteristics of the design in terms of area and timing, the noninvasive techniques suffer from low fault coverage and/or large test application times. Validation/functional testing methods start with a functional description of the circuit and make sure that the circuit's operation corresponds to its description. Various methods are geared towards extensive validation of the controller behavior of a given circuit under test.

Related Work

Various methods are implemented to detect the stuck- at fault in digital circuits.

Adding Buffer to each port of RTL Circuits.

The very first method is adding buffer to each ports of RTL circuits to create a new faulty circuit [7].

1. Firstly test bench is developed and the simulation is first run on a good circuit and then on each of the faulty circuits using any simulator.

2. The outputs obtained in each case of the faulty circuits are compared with the output of the good circuit to determine which faults are detected. That is the new faulty circuit and the fault free circuit is simulated and the outputs so obtained are compared. The fault list is tabulated.

3. The ratio of the numbers of RTL faults detected to the total number of RTL faults gives the RTL fault coverage.

In this work Virology Hardware Description Language is used for writing the RTL models. The basic assumption is that the components are fault free and only their interconnections are affected. These map to the operators and variables in the RTL descriptions respectively. Gate level primitives can be instantiated in a model

using gate instantiation as these are supported for synthesis.

These primitive gates describe the hardware. Therefore synthesizing a gate primitive generates logic based on the gate behavior which eventually gets mapped to the target technology .Based on this the single stuck-at fault is modeled. The assumption is also that at most one fault occurs at a time in the circuit.

The most common model used for logical fault is the single stuck-at fault (SSF). In this a fault in a logic gate gives a favourable outcome in one of its inputs or the output being fixed to either a logic 0(stuck-at-0) or a logic 1(stuck-at-1).

Next Method Is That In Which Validation Test Sets Are Used To Generate Test Sequences That Detect A Majority Of Stuck-At Faults In The Datapath[1].

1. The Scheme first derives the Controller Behaviors from Validation Test Sequences and Reuses Them for Simplifying Justification/ Propagation Analysis Corresponding to Precomputed test Vectors/Responses Of Datapath Rtl Modules.
2. A Heuristic Is Used To Identify Controller Behaviors That Are Compatible With A Given Set Of Precomputed Test Vectors/Responses. It Requires Only A Single Pass Through The Cdfg Corresponding To A Validation Test Sequence And Is Accu- Rate, Resulting In A Small Number Of Test Generation Runs.

3 Test Generation Is Performed at the Rtl and the Controller Behavior Is Prespecified, Which Results In Very Small L test Generation times. First Step Is

Table 1.RTL versus Gate-Level Fault Coverage

Name of the Circuit	**RTL Fault Coverage**	**Gate- Level Fault Coverage**
Full Adder	100%	100%
Multiplexer	100%	100%
Decoder	100%	100%
Comparator	100%	100%
Priority Encoder	100%	100%
JK Flip- Flop	100%	100%
D Flip- Flop	100%	100%

Identification of Compatible Controller Behaviors Consisting Of Augmented Fault Simulation to Derive Activation- Detection Time Frame Pair and Analysis Of Requirements To Identify Compatible Faults. Next Step Is Sat- Based Rtl Atpg Is Used To Obtain A Test Sequence That Reuses The Controller Behavior To Justify And Propagate The Precomputed Test Vector And Response To Primary Inputs And Outputs, Respectively. Sat- Based Rtl Atpg Uses An Ila Model Of The Circuit Under Test. The Circuit Is Unrolled For A Predetermined Number Of Cycles Determined By The Number Of Vectors In The Validation Test Sequence From Which The Controller Behavior Is Extracted. Test Generation Is Performed On the Entire Circuit Description Comprising The Controller And Datapath By first Identifying The Paths From The Inputs Of The Module Under Test To Primary Inputs And From The Output Of The Module Under Test To Primary Outputs In The Ila Model. These Paths Are Then Translated Into Boolean Clauses By Translating The Functionality Of The Individual Modules In These Paths. Once The Boolean Clauses That Capture The Rtl Test Generation Problem And The Controller Behavior Are Generated, A Sat Solver Is Invoked To Resolve These Clauses. If The Solver Returns With A Satisfiable Solution, Then A Test Sequence Can Be Extracted From The Boolean Variable Assignments Corresponding To The Primary Inputs.

Table 2. Reduction in Number of Test Generation Runsdue To the propose heuristics

Circuit	**Number of test generation runs**	
	Without heuristic (Worst Case)	**Without heuristic**
Sqr_mul	744	79
Sqr_add	1024	75
Exl	3605	156
Bessel	2133	105
Paulin	6027	193
ASPP4	6820	238
Parwan	3198	170

This Sequence Is Guaranteed To Deliver The Pre computed Test Vector To The Inputs Of The Corresponding Rtl Module And Propagate The Fault Effect From The Output Of The Module To A Primary Output. If The Boolean Clauses Are Not Satisfiable, Then Test Generation Fails, Indicating That The Targeted Precomputed Test Vector/Response Cannot Be Justified/Propagated By Reusing The Controller Behavior That Was Found To Be Compatible By Using The Heuristic.

Implementation of Automatic Test Pattern Generation.

Next method for detection of stuck-at fault consisting of an algorithm for generating test patterns automatically from functional register-transfer level (RTL) circuits that target detection of stuck-at faults in the circuit at the logic level.

In order to do this, a data structure named assignment decision diagram are used [5]. The algorithm is very versatile and can tackle almost any type of single- clock design, although performance varies according to the design style. The first step is to convert each process and concurrent RTL statements in each leaf component of the circuit into ADDs.

2. After that, each ADD is selected and its I nternals targeted for testing. First the arithmetic operations are targeted, then logic arrays, then untagged registers, latches, and memories, then untagged ADNs, and finally random logic blocks and black boxes.

1. ***Table 3.Test Generation Results***

Circuit	*HITEC*			*STRATEGATE*			*RTL ATPG*		
	FC (%)	TGen (sec)	TApp (cycles)	FC (%)	TGen (sec)	TApp (cycles)	FC (%)	TGen (sec)	TApp (cycles)
Paulin	97.92	147002	752	99.71	101071	4499	99.72	138	4124
Tseng	98.43	52139	366	99.63	18481	2689	99.68	216	3429
Dct	90.01	74805	1696	89.83	106056	2528	96.50	739	3965
GCD	49.16	43964	258	85.73	192384	55823	94.31	498	4568
Barcode	63.41	9799	759	57.58	232336	24764	88.78	876	4080
X25	36.31	93592	151	57.27	131897	20817	85.35	1046	3561
Am2910	73.86	18723	1317	94.48	15125	4742	95.32	2765	3952
GPIO	99.41	57	1396	98.30	11078	5292	93.56	5543	690
ALM	22.53	58600	589	29.53	67854	1563	36.52	85654	1430
EXE	21.32	27300	992	44.12	399333	26722	40.83	585700	5689

During testing of each RTL element, a nine-valued symbolic RTL justification and propagation is done to trace out paths from the PIs to the element inputs and element outputs to POs to obtain a symbolic test environment for the module. The search is a branch and bound type of search with backtracking and has a backtrack limit and search time limit that may be adjusted. It requires hierarchy traversal in case of a hierarchical design. The transformations across operations are based on the nine-valued RTL algebra and placed in a look-up table. If a search fails to obtain a test environment, then some heuristics are used to increase the coverage. Once the test environment is found, a precomputed test set is used (only for arithmetic operations) from a test set library to get a system-level test set for the RTL element. All system-level test sets for all RTL elements are concatenated together to get the complete RTL circuit test set.

CONCLUSIONS

It is observed that the RTL Fault Coverage obtained by the very first fault modeling methodology has a close match to the Gate-level Fault Coverage for the tested digital circuits. A novel approach is presented for using a validation test set to generate test sequences that have good stuck-at fault coverage for data path RTL modules. The scheme first derives the controller behaviors from validation test sequences and reuses them for simplifying justification /propagation analysis corresponding to precomputed test vectors/responses of data path RTL modules. A heuristic is used to identify controller behaviors that are compatible with a given set of precomputed test vectors/responses. It requires only a single pass through the CDFG corresponding to a validation test sequence and is accurate, resulting in a small number of test generation runs. Test generation is performed at the RTL and the controller behaviors prespecified, which results in very small test generation times.

A versatile RTL-ATPG algorithm is presented that can generate test vectors for almostany type of single-clock functional RTL design. The algorithm uses a data structure called ADD that helps it to tackle control and data flow in an unified fashion and a nine-valued algebra that helps it to do justification and propagation at the RTL. The algorithm degenerates to an inefficient logic-level ATPG algorithmic it is fed a Boolean network. The performance of the algorithm degenerates as the circuit description becomes more and more logic type. Current efforts are to

map effective logic-level ATPG heuristics into thealgorithm so that the performance is comparable to logic-level ATPG even for logic type designs.

Finally analyzing each and every methods which are mentioned above on the basis of fault coverage percentage, a suitable method will be implemented to improve the fault coverage of stuck-at fault to greater extend.

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