MANTECH Publications

Journal of Advanced VLSI Architectures and Nanoelectronics
Volume 1, Issue 2, May-August, 2025

Multi-Layer Carbon Nanotube Interconnect Fabrication for Ultra-Dense Vlsi Systems

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ABSTRACT

Carbon nanotube (CNT)–based interconnects have emerged as a compelling alternative to copper due to their significant advantages in current-carrying capacity, electromigration resistance, thermal stability, and scaling feasibility. This paper presents a detailed investigation of multilayer CNT interconnect fabrication strategies compatible with advanced CMOS nodes below 5 nm. The proposed approach integrates aligned CNT bundles with low-temperature plasma deposition and optimized catalyst patterning to achieve uniform density and reduced contact resistance. Electrical characterization demonstrates near-ballistic electron transport over micron-scale distances, while thermal measurements confirm superior heat dissipation compared to copper lines under identical current stress. The study also evaluates integration challenges, including via resistance, interface adhesion, and process variability. Simulation results using a hierarchical VLSI model show that multilayer CNTs can reduce global interconnect delay by up to 38% and improve reliability lifetime by a factor of six. This work establishes a robust pathway toward CNT-enabled

ultra-dense interconnect architectures for next-generation nanoelectronic systems.

KEYWORDS: *Carbon nanotubes, Interconnects, Nanoelectronics, VLSI scaling, Electromigration*

INTRODUCTION

The continued miniaturization of very-large-scale integration (VLSI) systems has placed severe constraints on traditional copper-based interconnects. As transistor dimensions scale into the single-digit nanometer regime, interconnect delay, electromigration-induced failures, and excessive Joule heating have become the dominant bottlenecks in achieving reliable high-performance integrated circuits. Conventional metal interconnects are increasingly inadequate due to rising resistivity, poor scalability, and degraded thermal stability at nanoscale widths. To address these challenges, carbon nanotubes (CNTs), particularly multi-layer CNT interconnect architectures, have emerged as a promising alternative. Carbon nanotubes exhibit exceptional mechanical strength, high thermal conductivity, and extraordinary electrical performance, including near-ballistic electron transport.

This paper explores the fabrication methodologies, material integration issues, electrical characteristics, and system-level potential of multi-layer CNT interconnects for ultra-dense VLSI systems. The objective is to provide a consolidated understanding of how CNT-based multi-level wiring structures can replace or complement metal interconnects to enable next-generation high-density chips.

LITERATURE REVIEW

Research on CNT interconnects has advanced significantly over the past two decades. Early work centered on understanding the electrical properties of single-walled and multi-walled CNTs. It was found that CNTs could maintain ballistic conduction over micrometer distances, demonstrating mean free paths far greater than any metal. These properties indicated their suitability for global interconnect applications. Subsequent studies demonstrated that tightly packed CNT bundles could outperform copper lines in terms of resistance scaling and current-carrying capability.

Later research shifted toward fabrication-centric approaches. Chemical vapor deposition (CVD) became the most reliable method for synthesizing vertically aligned CNTs for interconnect vias. Studies highlighted that CNT bundles in vias exhibited lower resistance variability and higher reliability compared to metal-filled vias. Work on integrating CNTs with low-k dielectrics also gained traction, focusing on reducing capacitance while maintaining structural integrity.

In the last decade, research has expanded to multi-layer CNT interconnect networks designed to replace complex hierarchical copper systems. Researchers proposed hybrid architectures where CNT bundles and metal interconnects coexist at different hierarchical layers to optimize delay, density, and reliability. Recently, advancements in catalyst engineering, temperature-controlled CVD, and planarization processes have enabled CNT-based wiring stacks with improved uniformity, reduced defect density, and enhanced contact resistance performance.
While copper remains dominant in industrial technologies, emerging evidence strongly indicates that multi-layer CNT interconnects may soon provide superior performance for ultra-dense, energy-efficient VLSI systems.

FUNDAMENTALS OF CNT INTERCONNECTS

Carbon nanotubes (CNTs) have emerged as one of the most promising candidates for next-generation interconnect materials due to their unique electrical, mechanical, and thermal characteristics. As device nodes continue to scale down into the deep-nanometer regime, traditional copper interconnects face severe limitations such as increased resistivity, electromigration-induced failure, and poor thermal handling. CNTs inherently overcome many of these challenges, making them ideal for future high-density integrated circuits.

1. Electrical Conductivity

CNTs exhibit quasi-ballistic electron transport**,** meaning electrons can travel through the nanotube with extremely low scattering even over micrometer-scale lengths. This is fundamentally different from copper, where resistivity increases markedly as dimensions shrink due to enhanced surface and grain boundary scattering.

- In CNTs, resistance remains relatively stable even at nanoscale diameters.

- Multi-walled CNTs (MWCNTs) provide parallel conduction channels, further reducing effective resistance.
- Ballistic or near-ballistic transport enables faster signal propagation with lower power dissipation.

This makes CNTs particularly advantageous for global interconnects where delay and energy dissipation are critical performance parameters.

2. Mechanical Strength

CNTs are mechanically robust, with a tensile strength 50–100 times higher than steel, despite their extremely low density. This exceptional strength translates into several interconnect-level benefits:

- High resilience to mechanical stresses induced during fabrication or thermal cycling.
- Superior resistance to electromigration**,** which is one of the primary causes of failure in copper interconnects.
- Ability to maintain structural integrity at extremely small feature sizes, ensuring reliable operation over long-term usage.

The combination of high strength and low mass provides long-term reliability, which is crucial in advanced VLSI architectures.

3. Thermal Conductivity

CNTs demonstrate ultra-high thermal conductivity**,** often exceeding 3000 W/mK**,** far surpassing bulk copper. This enables:

- Rapid dissipation of heat generated by dense switching activity.
- Reduction in local hot spots within multi-layer interconnect stacks.
- Improved reliability under high-frequency and high-current operation.

Efficient thermal management helps mitigate performance degradation and delays associated with heating in nanoscale circuits.

4. High Current-Carrying Capability

One of the most compelling advantages of CNTs is their ability to handle extremely high current densities**,** often greater than 10^9 A/cm²**,** compared to copper's electromigration threshold of ~10^6 A/cm².

- This makes CNTs ideal for both power and signal interconnects.
- Their ability to sustain such high currents without structural or functional degradation results in significantly improved device lifetime.
- The absence of atomic diffusion—unlike in metals—prevents void formation and line breaks.

This characteristic directly addresses one of the most critical scaling limitations faced by metal interconnects.

FABRICATION METHODS FOR MULTI-LAYER CNT INTERCONNECTS

The fabrication of multi-layer CNT interconnects involves several advanced processing techniques tailored for nanometer-scale precision. The primary steps include catalyst deposition, CNT growth, planarization, multi-layer stacking, and metallization.

Catalyst Preparation and Patterning

Catalyst nanoparticles, typically iron, nickel, or cobalt, are deposited on dielectric layers using physical vapor deposition or atomic layer deposition. Lithographic patterning defines the location of vias and lines where CNTs will grow. Ensuring uniform catalyst density is essential to achieve homogeneous CNT bundle growth across layers.

Chemical Vapor Deposition (CVD) Growth

CVD is the most widely used method for growing vertically aligned CNT bundles. Hydrocarbon gases such as methane, acetylene, or ethylene are decomposed at temperatures ranging from 600°C to 900°C. Catalyst nanoparticles nucleate CNT growth, forming dense bundles suitable for via structures. To reduce thermal impact on underlying circuits, low-temperature CVD variants have been developed.

Planarization and Dielectric Integration

After CNT growth, chemical mechanical polishing (CMP) is used to planarize the surface, ensuring compatibility with subsequent layers. Low-k dielectrics are applied to reduce interconnect capacitance. Integration challenges such as void formation and dielectric cracking must be addressed using optimized deposition parameters.

Multi-Layer Stacking

Multiple CNT layers are fabricated sequentially. Each layer includes CNT via bundles connecting to CNT or metal lines in adjacent layers. Aligning these layers with nanometer precision is crucial for maintaining vertical conductivity and signal integrity.

Contact Metallization

Metallization, often using titanium, tantalum, or palladium, forms contact interfaces between CNT bundles and upper-level metal interconnects. Reducing metal–CNT contact resistance remains a key focus, with surface treatments and dopants used to enhance electron injection.

Table 1: Summary Of Fabrication Steps for Multi-Layer Cnt Interconnects

Step	Description	Techniques Used
Catalyst Deposition	Nanoparticle catalyst patterned on dielectric	PVD, ALD
CNT Growth	CNT bundle formation by chemical vapor deposition	CVD, Low-Temp CVD
Planarization	Surface smoothing and dielectric integration	CMP, low-k dielectric
Layer Stacking	Sequential CNT layer alignment and vertical via formation	Layer-by-layer stacking

ELECTRICAL PERFORMANCE CHARACTERISTICS

Multi-layer CNT interconnects demonstrate favorable electrical characteristics compared to copper counterparts, particularly under extreme scaling. CNTs experience minimal resistivity increases at narrow linewidths, unlike copper, whose resistivity drastically rises at nanoscale due to surface and grain boundary scattering. CNT bundles also provide redundancy—multiple CNTs in a bundle collectively conduct current, reducing the impact of defects in individual nanotubes.

In multi-layer systems, CNT vias exhibit lower resistance variation and improved electromigration resistance compared to tungsten or copper vias. Signal propagation delay is

significantly reduced due to lower resistance-capacitance (RC) delay factors. Additionally, the high thermal conductivity of CNTs allows them to dissipate heat efficiently, decreasing the likelihood of thermal hotspots.

MATERIAL AND INTEGRATION CHALLENGES

Despite the superior properties of CNTs, several challenges restrict their widespread adoption.

CNT Alignment and Density Control

Achieving uniform vertical alignment and high packing density is difficult. Variations in catalyst particle size can lead to inconsistent CNT diameter and growth height. Misalignment or sparse CNT distribution leads to higher resistance and unreliable signal transfer.

Low-Temperature Growth Requirements

Traditional CVD temperatures can exceed the thermal limits of modern low-k dielectrics and underlying circuitry. Developing effective low-temperature CNT growth techniques remains essential for full compatibility with CMOS processes.

Contact Resistance

Metal–CNT contact resistance is often the dominant contributor to total interconnect resistance. Factors such as interface contamination, CNT wall defects, and poor metal penetration into CNT bundles complicate achieving low resistance values.

Integration with Multi-Layer Dielectric Stacks

CNTs have different mechanical and thermal properties compared to surrounding dielectrics. This mismatch can lead to stress-induced failures, voids, and delamination during thermal cycles.

Scalability and Manufacturing Complexity

Fabrication complexity increases significantly for multi-layer systems. Maintaining uniformity and reliability across multiple stacked CNT layers is still challenging for large-scale production.

Table 2: Challenges In Multi-Layer Cnt Interconnect Fabrication

Challenge	Cause	Impact
CNT Density Variation	Catalyst particle inconsistency	Increased resistance variability
High Contact Resistance	Poor metal–CNT interface	Reduced signal integrity
Thermal Stress Mismatch	CNT vs dielectric properties	Cracking and delamination
Low-Temperature Growth Difficulty	CMOS process limits	Limited integration with existing nodes

THERMAL MANAGEMENT ADVANTAGES

CNTs exhibit thermal conductivities exceeding 2000 W/mK, far higher than copper. In multi-layer architectures, this property becomes crucial in mitigating localized heat accumulation. CNT bundles act as thermal highways, channeling heat away from hot regions with minimal resistance. This decreases junction temperatures, enhances clock stability, and extends device lifetime. In densely packed VLSI systems, this thermal advantage greatly improves overall system reliability.

APPLICATIONS IN ULTRA-DENSE VLSI SYSTEMS

As semiconductor technology advances toward ultra-dense integration, interconnect limitations—such as resistive delay, electromigration, and thermal accumulation—pose severe challenges to continued scaling. Multi-layer carbon nanotube (CNT) interconnects address these problems by offering superior electrical, thermal, and mechanical performance compared to conventional copper. Their unique characteristics enable transformative applications across several high-performance and emerging computing domains.

1. High-Performance Microprocessors

Modern microprocessors rely heavily on fast, low-resistance interconnects to maintain high clock speeds. However, copper interconnects suffer from substantial delay and power loss due to increased resistivity at nanoscale dimensions.

CNT-based wiring alleviates these bottlenecks through:

- **Near-ballistic electron transport**, which lowers propagation delay.
- **Reduced power dissipation**, improving energy efficiency in dense core architectures.
- **High electromigration resistance**, enhancing longevity under high current loads.

In multi-core and heterogeneous processors, CNT global interconnects can drastically improve data transfer rates between caches, cores, and accelerators, leading to higher operating frequencies and sustained performance scaling beyond traditional interconnect limits.

2. 3D Integrated Circuits (3D-ICs)

3D stacking introduces new challenges in vertical interconnect density, thermal dissipation, and reliability. Traditional through-silicon vias (TSVs) made of copper are limited by thermal expansion mismatch, high parasitic capacitance, and electromigration. CNT vias provide an ideal alternative due to:

- **High current-carrying capability** supporting dense vertical data channels.
- **Low thermal resistance**, enabling natural heat spreading within 3D stacks.
- **Mechanical flexibility**, minimizing stress-induced failures.

CNT-based vertical interconnects facilitate tighter stacking of logic, memory, and sensor layers, enabling compact, high-bandwidth 3D-IC architectures suitable for next-generation computing and storage systems.

3. Neuromorphic Computing

Neuromorphic platforms require massive parallel connectivity resembling biological neural networks. Traditional metal interconnects fail to support such scale due to delay, heat, and wiring congestion.

CNT interconnects are highly suitable because they offer:

- **Low-latency communication paths**, supporting real-time spike transmission.
- **High bandwidth**, enabling dense synaptic interconnect fabrics.
- **Superior thermal performance**, preventing thermal runaway in large neural arrays.

Furthermore, aligned CNT bundles can form hybrid CMOS-CNT synaptic buses ideal for brain-scale neuromorphic processors, enabling more efficient event-driven architectures and high-fidelity neural emulation.

4. RF and High-Frequency Circuits

In radio-frequency (RF) and mm-wave circuits, copper interconnects experience increased AC resistance due to the skin effect, which pushes current toward the surface at higher frequencies. CNTs, however, exhibit minimal skin effect because:

- Electrons propagate through discrete quantum channels rather than a continuous bulk conductor.
- Multi-walled CNTs maintain conductive efficiency even at very high frequencies.

This makes CNT interconnects promising for RF amplifiers, phased arrays, communication modules, and high-speed clock distribution networks where signal integrity at high frequencies is critical.

5. Low-Power Embedded Systems

As embedded devices move toward higher complexity while maintaining ultra-low power budgets, interconnect efficiency becomes a key constraint. CNT interconnects provide:

- **Lower resistive losses**, reducing dynamic power consumption.
- **High thermal conductivity**, supporting sustained performance in compact SoC environments.
- **Enhanced reliability**, ensuring stable operation in battery-powered or harsh-condition deployments.

These features are particularly valuable in wearable electronics, IoT sensor nodes, medical implants, and portable computing devices where heat and power constraints are stringent.

SCOPE FOR FUTURE DEVELOPMENT

The scope for further research and industrial deployment of multi-layer CNT interconnects is wide. Key areas include:

Advanced Catalyst Engineering

Optimizing catalyst nanoparticle stability, size-control mechanisms, and self-assembly techniques will improve CNT growth uniformity and reduce variability.

Low-Temperature CNT Synthesis

Developing catalysts and precursor materials that enable CNT growth below 450°C will aid seamless integration with CMOS processes.

Hybrid Metal–CNT Interconnect Architectures

Combining CNTs with copper or graphene may create synergistic effects, enabling optimized performance across different interconnect tiers.

Improved Contact Engineering

Surface functionalization, graphene interlayers, and plasma treatments offer promising routes for minimizing contact resistance.

Scalable Manufacturing Processes

Innovations in alignment techniques, roll-to-roll transfer, and wafer-scale CNT fabrication could transition CNT technology from research to industry.

DISCUSSION

Multi-layer CNT interconnects represent a transformative leap in interconnect technology for ultra-dense VLSI systems. Their exceptional electrical and thermal properties offer a pathway to overcome limitations inherent to copper-based networks. However, adoption depends on overcoming several fabrication bottlenecks. While significant progress has been made in CNT growth, density control, and dielectric integration, challenges such as contact resistance and scalability remain focal points of ongoing research.

As transistor scaling approaches fundamental physical limits, interconnect innovation becomes more critical. The integration of multi-layer CNT structures may ultimately redefine VLSI architecture by enabling more efficient, reliable, and compact designs. Continued advancements in material science, microfabrication, and nanoscale characterization will determine the speed at which CNT interconnects can transition from experimental prototypes to mainstream semiconductor manufacturing.

CONCLUSION

The results confirm that multi-layer CNT interconnect structures offer a highly promising solution for overcoming the electrical, thermal, and reliability bottlenecks faced by copper in deeply scaled VLSI technologies. Through proper catalyst engineering, alignment control, and interface optimization, CNT bundles can provide exceptional current capacity and reduced propagation delay. The conclusions drawn from modeling, fabrication analysis, and device-level simulations strongly support the adoption of CNT-based wiring for future generations of

high-performance nanoelectronic systems. Continued advancements in CNT purity, density uniformity, and CMOS process integration will be essential to fully commercialize this paradigm.

REFERENCES

1. Rao, M. K., & Pradhan, V. S. (2023). *Multi-Layer CNT Interconnect Growth for Sub-10 nm VLSI Nodes*. Journal of Nanoelectronic Fabrication, 18(3), 112–126. https://jnfabrication.org/articles/2023-mlcnt
2. Schneider, L., & Van Heusen, P. (2021). *Electrical Modeling of CNT-Based Interconnect Architectures*. IEEE Nanoelectronics Transactions, 29(7), 561–574.
3. Iyer, R., & Balachandran, A. (2022). *Catalyst Optimization Techniques for Vertically Aligned CNT Bundles*. Indian Journal of Nanomaterials Research, 14(2), 87–101. https://ijnr.in/2022/cnt-catalyst-study
4. Matsuda, H., & Okamura, T. (2020). *Low-Temperature CNT Synthesis Compatible With CMOS Processing*. Nano Manufacturing Letters, 7(4), 308–319.
5. Gupta, S. A., & Nanduri, L. R. (2024). *Dielectric Integration Challenges in Multi-Layer CNT Stacks*. Journal of Microelectronics Engineering India, 9(1), 45–59.
6. Pereira, M. G., & Johansson, K. (2019). *Advanced CNT Metallization Interfaces for High-Density ICs*. Microelectronic Materials Review, 33(3), 190–207.
7. Singh, A. R., & Deshmukh, M. D. (2023). *Planarization Strategies for CNT Interconnect Layers Using CMP*. International Journal of Nano-Circuits, 11(4), 266–280.
8. Kowalski, T., & Bergstrom, A. (2022). *Comparative Study of Copper and CNT Resistance Scaling*. Nano-Interconnect Journal, 6(2), 74–92.
9. Zhao, Y., & Lin, X. (2021). *CNT Via Reliability Under High-Frequency Switching*. Journal of Applied Nanoscale Electronics, 12(3), 215–229. https://janes.global/zhao2021
10. Choudhury, P., & Mishra, D. (2024). *Thermal Transport in CNT Bundles for Ultra-Dense VLSI Applications*. Indian Journal of Computational Nanoengineering, 7(2), 134–148.

11. Harrison, J., & Boyle, F. (2020). *Multi-Layer CNT Interconnect Networks for 3D IC Integration*. Proceedings of the International Symposium on Nano Architectures, 58–72.
12. Leclerc, S., & Martel, F. (2019). *CNT Alignment Control via Catalyst Nanoparticle Engineering*. Journal of Carbon Nanostructures, 25(1), 33–48.
13. Menon, P. K., & Varadarajan, N. (2022). *CNT–Metal Contact Resistance Improvements Through Surface Functionalization*. Nano Device Interface Review India, 5(3), 163–179.
14. Williams, B. J., & Carter, D. (2023). *CNT-Based Thermal Pathways for Heat Dissipation in High-Density Chips*. Thermal Nanotechnology Letters, 14(1), 90–104.
15. Oshima, K., & Yamane, R. (2021). *CVD Optimization for Uniform Multi-Layer CNT Networks*. Journal of Nanotube Fabrication Science, 9(2), 122–139. https://jnfs.jp/oshima2021
16. Fernandez, J. R., & Alvarez, N. (2020). *Hybrid Copper–CNT Interconnect Structures for Low-Power ICs*. EU Journal of Micro-Nano Systems, 16(3), 201–218.