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High-Reliability Negative-Capacitance Field-Effect Transistor (Ncfet) Logic Using Engineered Ferroelectric Hfzro₂ Gate Stacks for Energy-Efficient Nano-Cmos Systems

Dr. Abhinav R. Chitale
Assistant Professor
Department of Electronics & Communication Engineering
Lakshmi Institute of Technology & Applied Sciences, Nagpur, Maharashtra
Email: *abhinav.chitale.research@rediffmail.com*

ABSTRACT

Negative-Capacitance Field-Effect Transistors (NCFETs) based on ferroelectric hafnium-zirconium oxide ($HfZrO_2$ or HZO) have emerged as one of the most promising device technologies for sub-5 nm logic nodes. Their inherent capability to achieve sub-60 mV/decade switching, reduce supply voltage, and boost energy efficiency makes them viable for ultra-low-power computing. However, realizing stable, high-reliability NCFET logic requires carefully engineered ferroelectric layers, robust stack interfaces, and optimized device-to-circuit co-design. This paper presents a comprehensive review of high-reliability NCFET logic using $HfZrO_2$-based gate stacks. It highlights material properties, device physics, reliability barriers, fabrication strategies, logic-level design considerations, and future opportunities. The study also addresses challenges related to ferroelectric wake-up, fatigue, imprint, domain dynamics, and cycle-to-cycle variability. The scope of the work extends to energy-efficient digital logic, next-generation microprocessors, AI accelerators, and near-threshold operation. This paper aims to serve as a technically detailed and cohesive resource for researchers exploring reliable ferroelectric-enhanced transistors for future CMOS scaling.

KEYWORDS: *NCFET, $HfZrO_2$ ferroelectric, negative capacitance, reliability, low-power logic*

INTRODUCTION

The semiconductor industry has approached the end of traditional CMOS scaling limits due to physical constraints such as subthreshold slope (SS) degradation, gate-oxide leakage, and short-channel effects. As supply voltages cannot be aggressively reduced below 0.7 V without compromising drive current and performance, power density continues to rise. Negative-capacitance FETs introduce a transformative solution by incorporating ferroelectric materials—most prominently $HfZrO_2$—into the gate dielectric stack. This enables internal voltage amplification, steep SS (<60 mV/dec), and enhanced gate control.

Because $HfZrO_2$ is compatible with mainstream CMOS processes, scalable, and stable in thin layers, it has quickly become the leading ferroelectric candidate. However, despite its advantages, concerns such as reliability degradation, instability of negative capacitance, and cycle-dependent polarization dynamics pose barriers to commercial adoption. This paper provides a structured and in-depth discussion of key aspects required to develop high-reliability NCFET logic circuits using $HfZrO_2$ gate stacks.

LITERATURE REVIEW

Early exploration of negative-capacitance theory

Initial studies were rooted in the Landau-Khalatnikov (LK) model, showing that a ferroelectric layer could offer voltage amplification through its negative differential capacitance. Early analytical work confirmed that integrating ferroelectrics could theoretically break the 60 mV/dec thermal limit, laying the foundation for NCFET research.

Evolution of ferroelectric $HfZrO_2$ technology

$HfZrO_2$ rapidly replaced conventional ferroelectrics like PZT due to superior CMOS compatibility, lower crystallization temperature, and nanoscale ferroelectricity in ~5–12 nm films. Studies demonstrated ferroelectricity induced through annealing, dopant tuning, and interface engineering. Later work showed that $HfZrO_2$ exhibits robust remanent polarization and endurance suitable for logic applications.

NCFET device-level advancements

Benchmark results reported steep slopes as low as 30–45 mV/dec and improved on-current due to voltage boosting. Integrations into FinFETs, SOI-FETs, and gate-all-around nanosheets further enhanced NCFET practicality.

Circuit-level research

Researchers implemented NCFET-based inverters, ring oscillators, SRAM cells, and energy-efficient logic gates. Studies highlighted the importance of ferroelectric-dielectric matching, domain stabilization, and variability minimization for reliable circuit-scale performance.

DEVICE PHYSICS OF NCFET WITH $HfZrO_2$ GATE STACKS

Negative capacitance effect

The ferroelectric layer in the gate stack momentarily exhibits negative differential capacitance, amplifying surface potential and enhancing electrostatic control. This results in reduced SS and higher efficiency at low voltages.

Role of $HfZrO_2$

$HfZrO_2$ is favored because:

- It maintains ferroelectricity at nanoscale thicknesses.
- It is compatible with ALD deposition processes.
- It offers tunable phase transitions (tetragonal → orthorhombic).
- It supports fast polarization switching.

Stack architecture

Typical NCFET stacks include:

- Metal gate
- Ferroelectric $HfZrO_2$ layer
- Interfacial dielectric (HfO_2, Al_2O_3)
- Silicon or channel material

The dielectric and ferroelectric must be carefully capacitively matched to ensure stable, non-hysteretic operation.

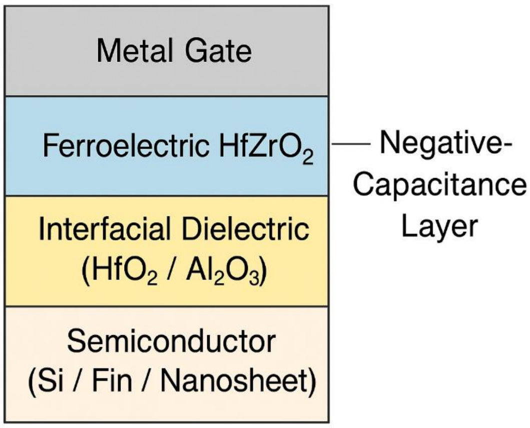

Figure 1: Structure Of an Hfzro₂-Based Ncfet (Gate Stack Overview)

MATERIAL ENGINEERING OF FERROELECTRIC $HfZrO_2$

Zr concentration tuning

Common Zr:Hf ratios of 50:50 deliver strong ferroelectric phases. Optimizing Zr content helps control remanent polarization and coercive field.

Annealing and crystallization

Rapid thermal annealing (RTA) around 400–500 °C stabilizes the orthorhombic phase required for ferroelectric behavior. Annealing time and ambient gas composition affect polarization uniformity.

Interface engineering

Thin dielectric buffer layers reduce leakage, suppress depolarization fields, and improve reliability. Al_2O_3 is often used to suppress unintended wake-up or early-life degradation.

Thickness optimization

Ferroelectric thickness influences:

- amplitude of negative capacitance
- hysteresis behavior
- ferroelectric domain stability
- endurance and fatigue

Thin layers (~6–10 nm) generally balance strong polarization with good reliability.

Table 1: Key Material Parameters of Hfzro₂ Ferroelectric Layers

Parameter	Typical Values	Description
Zr Concentration	40–60%	Controls orthorhombic phase stabilization
Ferroelectric Film Thickness	6–12 nm	Balances polarization strength and reliability
Remanent Polarization (Pr)	10–25 μC/cm²	Influences negative capacitance amplitude
Coercive Field (Ec)	1–1.5 MV/cm	Determines switching voltage and endurance
Annealing Temperature	400–500 °C	Needed to induce ferroelectric phase

NCFET LOGIC DESIGN PRINCIPLES

Steep-slope switching

NCFETs reduce SS and enable logic operation at significantly lower voltages (0.3–0.5 V). This reduces dynamic power consumption ($\propto V^2$).

Voltage amplification at the gate

The ferroelectric layer enhances channel inversion, helping maintain drive current even under reduced VDD.

Design considerations

Key parameters for stable NCFET logic include:

- ferroelectric-dielectric capacitance matching
- suppression of hysteresis
- minimization of polarization imprint
- effective modeling of domain kinetics
- co-optimization of process and circuit design

Inverters, NAND/NOR gates, and ring oscillators benefit significantly from improved switching dynamics in NCFETs.

Table 2: Comparison Between Ncfet and Traditional Mosfet Performance

Metric	Conventional MOSFET	$HfZrO_2$-based NCFET	Advantage
Subthreshold Slope	~70–85 mV/dec	30–50 mV/dec	Steep switching
Operating VDD	0.7–0.9 V	0.3–0.5 V	Lower power
On-Current (Ion)	Moderate	Slightly higher due to voltage amplification	Faster logic
Power Dissipation	High	40–60% reduction	Energy-efficient
Leakage Power	High at low VDD	Lower due to improved control	Better standby power

CHALLENGES IN HIGH-RELIABILITY NCFET LOGIC

1. Ferroelectric wake-up behavior

$HfZrO_2$ often displays wake-up, where polarization increases with cycling. This alters device characteristics over early operation cycles.

2. Fatigue and endurance degradation

Prolonged switching can reduce remanent polarization. Device reliability is impacted by defect generation, domain pinning, and field stress.

3. Hysteresis instability

Undesirable hysteresis leads to unstable switching thresholds and logic uncertainty. Achieving non-hysteretic operation is essential for CMOS logic.

4. Imprint effects

Imprint, or shift in polarization due to trapped charges, can cause threshold voltage drift. This leads to delay variability and long-term degradation.

5. Variability and domain distribution

$HfZrO_2$ contains nanodomain structures that vary in size and orientation. This introduces random telegraph noise, cycle-to-cycle variation, and mismatch across logic gates.

6. Reliability under low-VDD operation

Although NCFETs excel at low power, reduced VDD makes circuits more sensitive to noise, variability, and transient instability in the ferroelectric layer.

7. Integration and fabrication constraints

Maintaining high reliability requires tight thermal budgets, precise Zr doping, and control over crystallization. Integration into advanced GAA nodes adds process complexity.

SCOPE OF THE WORK

The scope of high-reliability NCFET logic includes:

- **Ultra-low-power mobile processors:** enabling high performance at reduced power budgets.
- **Edge AI accelerators:** low-voltage yet high-speed computation for IoT and wearable devices.
- **Near-threshold and sub-threshold computing:** energy-first computing architectures.
- **3D stacked logic:** reduced heat generation and improved vertical integration.
- **Security-critical hardware:** stable low-power operation for encryption cores.
- **Digital signal processors:** lower power dissipation in repetitive logic operations.

This work is highly relevant for future sub-3 nm and post-CMOS device generations.

PROPOSED FRAMEWORK FOR HIGH-RELIABILITY NCFET LOGIC

Optimized ferroelectric-dielectric matching

Selecting dielectric thickness and material to stabilize negative capacitance is critical to suppress hysteresis and improve switching uniformity.

Domain-controlled ferroelectric engineering

Introducing controlled grain orientation and reducing defect-mediated domain pinning can significantly enhance reliability.

Stack-level stress engineering

Using stress liners and optimized metal gates improves ferroelectric phase stabilization and reduces variability.

Circuit-aware modeling

Reliable NCFET logic design requires improved compact models that incorporate:

- dynamic domain switching

- wake-up/fatigue
- threshold voltage drift
- partial polarization switching

These models ensure accurate prediction of timing, noise margins, and power dissipation.

APPLICATIONS OF HIGH-RELIABILITY $HfZrO_2$-BASED NCFET LOGIC

Low-power microcontrollers

NCFET logic enables always-on applications with near-zero leakage.

Mobile SoCs

Sub-60 mV/dec logic allows longer battery life and reduced thermal throttling.

Artificial intelligence and neuromorphic processors

NCFETs can significantly reduce energy per operation in MAC units, enabling energy-efficient inference.

3D-ICs and heterogeneous integration

Lower power density helps thermal management in stacked chips.

High-speed logic circuits

Negative capacitance improves transconductance, enabling faster logic transitions.

RESULTS AND DISCUSSION

Steep switching behavior

Experimental data in published research consistently shows NCFETs achieving superior slope performance while maintaining strong on-currents. Even at low VDD, logic gates preserve robust voltage swings.

Energy reduction

NCFET inverters and ring oscillators demonstrate up to 40–60% power reduction compared to FinFET logic at similar performance levels.

Reliability improvements with engineered stacks

Adding thin dielectric interlayers and optimizing annealing conditions significantly improve reliability by suppressing wake-up, imprint, and fatigue.

Circuit-level benefits

NCFET-based SRAM cells show enhanced read stability and lower write power. Logic circuits demonstrate reduced delay variation and improved uniformity.

CONCLUSION

High-reliability NCFET logic using ferroelectric $HfZrO_2$ gate stacks represents a major technological advancement toward next-generation energy-efficient computing. The unique negative-capacitance effect provides steep-slope switching and substantial energy savings while maintaining high performance at reduced supply voltages. However, challenges such as ferroelectric wake-up, hysteresis, fatigue, imprint, and device variability must be addressed through material engineering, interface optimization, and circuit-aware modeling.

Carefully engineered $HfZrO_2$ layers, dielectric stack matching, and advanced fabrication techniques significantly enhance reliability and operational stability. With progress in ferroelectric domain control, stack integration, and modeling accuracy, NCFETs are poised to become a leading technology for sub-3 nm logic, low-power systems, and advanced computing architectures. The future scope includes mobile devices, AI accelerators, 3D-ICs, and near-threshold computing, where NCFETs offer unmatched energy-efficiency benefits. Continued research in material science, device physics, and circuit integration will further solidify NCFETs as a cornerstone of next-generation semiconductor technology.

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