Implementation of All-Optical Even Parity Checker Using the Micro-Ring Resonator Structure

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Abstract

The Diverse field of all-optical computing technique provides the door of very efficient high-speed signal processing, which includes some considerable advantages of optical communication e. g. miniature size, secure transmission, less attenuation, greater bandwidth, and less computation time. The proposed paper describes the concept of switching activity of Micro-Ring resonator (MRR)and Further, the switching activity of MRRs is efficiently applied to implement the 4 bit all-optical even parity checker. The appropriate layout diagram along with the mathematical aspects of the proposed device is described in this paper. The discussed schemes are verified and simulated using MATLAB.

Keywords: - *MRR, All-optical logic gates, All-optical parity checker.*

INTRODUCTION

The modern era communication technology focused innovative and optimum methodology to improve the communication system. Implementation of digital computing phenomena is one of the most important aspects, which includes some considerable advantages of optics. Many researchers have achieved an accurate switching activity, where the switching activities are further utilized to explore the concepts of various combinational and sequential activities. In many cases, the idea of linear electro-optic effect (EO effect) (Pockels effect) is applied for the improved switching activity. One of the concepts of signal selectivity in the form of 1×4 optical signal router is discussed in [1]. The paper discusses an overview of the integrated optical signal router based on the concept of the EO effect. Similarly, many researchers have employed the optical interferometer circuits, which is a combination of optical couplers and optical delay devices, which are a common element employed in all-optical devices [2]-[4]. Based on the EO effect and proper feedback mechanism, the implementation of sequential circuitsis investigated [5]. Using the principle of linear EO effect, some work has been explored to observe some combinational logical phenomena. Using the concept of Pockels effect the concept associated with basic logic gate [6]-[8], optical universal logic gates, and some MOEMS pressure sensors [9] are widely investigated. However, all the switching activities associated with [1] and [5]-[9] are based on the concept of the EO effect, where the semiconductor optical amplifier (SOA) is not used for the implementation of logical functionality. In the same manner, many researchers are also involved with some other techniques to implement the function of sequential logic. The implementation and performance of two optical latchesand flip-flops have been studied in [10], [20]. A novel design of some all-optical circuits that can be involved for the functions realizing multi-valued logic is described in [11]. Similarly,a novel architecture of an all-optical flip-flop is proposed [12]. The architecture includes the single semiconductor optical amplifier-based Mach-Zehnder interferometer having a feedback loop. With thesimulation result, it may achieve low switching energies and fast operation. The novel scheme for an all-optical various sequential circuits and programmable logic devices having very low complexity has been investigated [13], [14], [15]and [17].[16] have been suggested and described a novel all-optical memory device to store ultra-speed optical data transfer for the long term.[18] have beenimplemented a broad-band all-optical flip-flop for the WDM system consists of optical bi-stability in an (SOA). In our proposed work it has been described as an approach to implement the all-optical even parity checker. In

Section-I, we discussed the introduction earlier relevant works associated with the technology, and second sectiondesignates the important mathematical formulations behind MRR based switching phenomenon. In third section, we designed and analysed the techniques to implementthe 4 bit all-optical even parity checkercircuit with its complete layout diagram. The discussed schemes are verified and simulated using MATLAB. Finally, we describe the conclusion in section IV

Micro-Ring Resonator

The MRR is one of the optical switching device, most of the researchers forthe switching phenomenon in optical domain are focused on coupling principle between the I/O optical waveguide with the optical ring resonator. For that MRR comprises the optical ring resonator, i.e., the mechanism based on resonator cavity. A portion of continuous-wave signal or logical data ispermitted to transmit to the ringresonator, fig. 1 shows the details. k_1 is the coupling coefficient of the input optical waveguide with the optical ring resonator and r is the radius of the optical ring resonator. It has been observed that the positive interference may be occurred, if it is the total optical path length is a multiple of wave-lengths. The positive interference in MRR is known as "ON RESONANCE". So the output port of the MRR provides fringes periodic in nature. Thecoupling coefficient of the optical ring resonator with the output optical waveguideis k_2. The developed wave inner ring is coupled to the output port, provides the maximum transmission in drop ports.

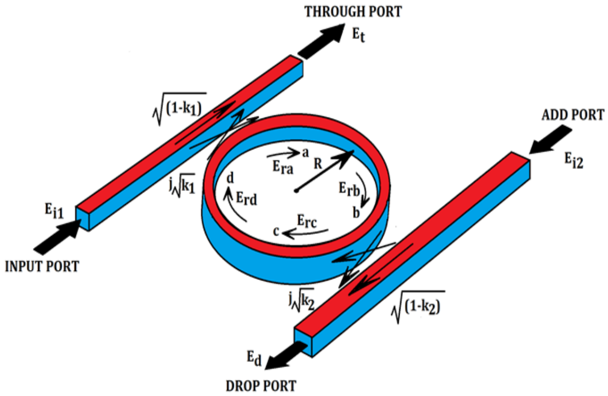

Fig 1: Single microring resonator

As a result, the through ports have minimum resonance. For the proper switching activity, the non-linear substantial hasbeen used to produce the resonance. By applying theproper light amplitude through the ring resonator form the top of ring excitation is observed in the optical ring and the effective index is varied. And finally, the refractive index may comparable decrease due to high-density carrier generated from the total absorption of intensity, which makes the blue-shift phenomenon, momentarily for the particular micro-resonance wavelengths. Different resonant wavelength occurs due to variation in the refractive index (R.I) then this phenomenon is used as switching activity for ON or OFF for a signal Considering L is the circumference of the optical ring . k_1 Is the coupling coefficient of the input optical waveguide with the optical ring resonatorwhereascoupling coefficient of the optical ring resonator with the output optical waveguide is k_2, intensity attenuation coefficients of the optical ring is α, $\gamma$is the intensity insertion loss coefficients andwave propagation constantis k_n, where $k_n = \frac{2\pi}{\lambda} n_{eff}$, the resonant wavelength of the ring is λ. $n_{eff} = n_0 + n_2.I = n_0 + \frac{n_2}{A_{eff}} P$, where $n_0$is linear R.I and n_2 are nonlinear R.I. in an optical pump, signal intensity is I and power is denoted by P. Let usconsider $E_{i1}$is input port field and $E_{i2}$is the add port field. In the optical ring the field at different points named as a, b, c, and d are E_{ra}, E_{rb}, E_{rc}, and E_{rd} respectively can be written as [11, 19, and 21],

$$E_{ra} = (1-\gamma)^{1/2}\left[j\sqrt{k_1}E_{i1} + \sqrt{(1-k_1)}E_{rd}\right] \quad (1)$$

$$E_{rb} = E_{ra}\exp(-\alpha L/4)\exp(j\,k_n L/2) \quad (2)$$

$$E_{rc} = (1-\gamma)^{1/2}\left[j\sqrt{k_2}E_{i2} + \sqrt{(1-k_2)}E_{rb}\right] \quad (3)$$

$$E_{rd} = E_{rc}\exp(-\alpha L/4)\exp(j\,k_n L/2) \quad (4)$$

The through port field is given by

$$E_t = (1-\gamma)^{1/2}\left[\sqrt{(1-\ k_1)}E_{i1} + j\sqrt{k_1}E_{rd}\right] \quad (5)$$

The drop portfield is given by

$$E_d = (1-\gamma)^{1/2}\left[\sqrt{(1-\ k_2)}E_{i2} + j\sqrt{k_2}E_{rb}\right] \quad (6)$$

For the generalization it is assumed,

$$D = (1-\gamma)^{1/2},\ \ x = D\exp\left(-\alpha\frac{L}{4}\right)\text{And}\phi = \frac{k_n L}{2}$$

By Solving Eq. (1) - (6), we developthe E_t(TP)and the E_d(DP) field as:

$$E_t = \frac{D\sqrt{1-k_1} - D\sqrt{1-\ k_2}x^2\exp^2(j\phi)}{1-\ \sqrt{1-k_1}\sqrt{1-\ k_2}x^2\exp^2(j\phi)}E_{i1} + \frac{-D\sqrt{k_1 k_2}x\exp(j\phi)}{1-\ \sqrt{1-k_1}\sqrt{1-\ k_2}x^2\exp^2(j\phi)}E_{i2} \quad (7)$$

$$E_d = \frac{-D\sqrt{k_1k_2}x\exp(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i1} + \frac{D\sqrt{1-k_1}-D\sqrt{1-k_2}x^2\exp^2(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i2} \quad (8)$$

Thegeneralizedequations E_t *and* E_d are the key terms for switching activity in ring resonator and helps in various design and analysis for any combinational and sequential logic circuits. It also assists to design the cascaded ring resonator. Thecascaded structurefor GaAs-AlGaAs basedMRR is done having wavelength(λ) for the COS input and having without any input in add port. Considering Coupling co-efficient$K_s = 0.25$,$(\alpha) = 0.0005\,\mu m^{-1}$, effective cross-sectional area = $0.25\,\mu m^2$ and the $\lambda = 1.55\,\mu m$.

Design of all-optical parity checker using the MRR structure

In the data transmission system, binary data is transmitted from source to destination, the error may occur in the transmitted data. Therefore, it is necessary to know the status of the error at the receiver end.In other words, the receiver should be able to know whether the received information is having an error or not. To detect such type of error, the parity check method is used wherein one extra bit called the parity bit is added with the information bit at the transmitter side to make the total number of 1s in the data-word either even or odd. If the number of 1s in the data-word is even then it is called the even parity check method and when the number of 1s in the data-word is odd then it is named the odd parity check method. In the even parity data transmission method, if the number of 1s in the data received at the receiver side is odd then it indicates that error has occurred and if the number of 1s in received information is even, it shows there is no error. Similarly, for the odd parity method, an odd number of 1s in the received data indicates no error but an even number of 1s in the received information shows the presence of error. The parity check phenomenon is having the restriction that it can detect only a single bit error. The circuit that produces the parity bit at the transmission side is named Parity Generator and the circuit that produces the parity at the receiver end is named Parity Checker. As our objective in this paper is confined with the implementation of the parity checker part only so, let us consider the truth table of a 4 bit even parity checker which is represented in table 1 below.

Table 1: Truth Table of 4 bit even parity checker

b_3	b_2	b_1	b_0	P (Even Parity)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Based on the truth table of even parity checkers, it shows that if the number received 1's is odd then an error will arise. Hence, table 1 can be used to calculate K-Map analysis and appropriate digital circuit as shown in fig. 2.

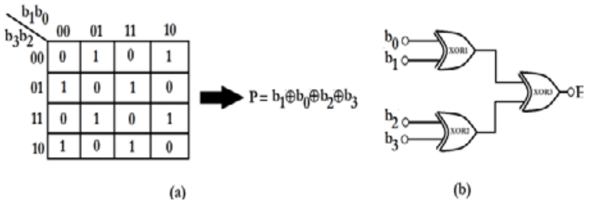

Fig 2: 4 bit even parity checker (a) K-map (b) Circuit diagram

Now, the suitable layout diagram describing the all-optical implementation of 4 bit even parity checker can be signified in the fig. 3. Fig 3 explores the basic layout diagram of all-optical 4 bit even parity checker using the proper configuration of 6 identical MRR structure. The input port of the MRR1, MRR3, and MRR5 the Continuous optical signal (COS) with the wavelength $\lambda = 1.55\,\mu m$ is applied. Thecascaded arrangement of MRR1 and MRR2 provides the XOR functionality at the drop port of the MRR2, where MRR1 as well as MRR2 is modulated through the optical control pump signal b_0 and b_1, respectively [22]. Hence, the MRR1 and MRR2 provide the optical equivalent of b_0 XOR b_1. Thus, it can be termed as g_0. In a similar manner, optical control pump signal b_2 and b_3 are applied to the specific arrangement of MRR3 and MRR4, respectively. Hence, we can generate the b_2 XOR b_3 optically at the drop port of the MRR4, which can be termed as the g_1.

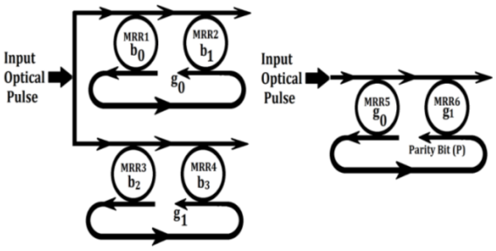

Fig. 3: The Layout of All-Optical 4 Bit Even Parity Checker using the 6 identical MRR structures

Finally, optical signalg_0 and g_1 acts as the input control pulse for the MRR5 and MRR6, respectively. The cascaded configuration of the MRR5 and MRR6 provides the optical pulse equal to the g_0 XOR g_1, which can be treated like the optical even parity checker bit. The proposed structure is simulated using MATLAB software. The appropriate simulated result using MATLAB is as follow:

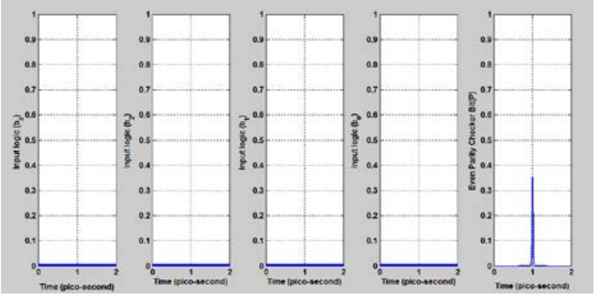

Fig. 4: Simulated result using MATLABfor the proposed 4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0000, which shows the corresponding even parity checker bit as '0'

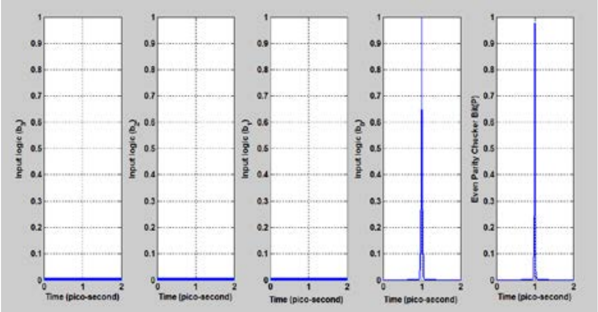

Fig. 5:Simulated result using MATLABfor the proposed 4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0001, which shows the corresponding even parity checker bit as '1'.

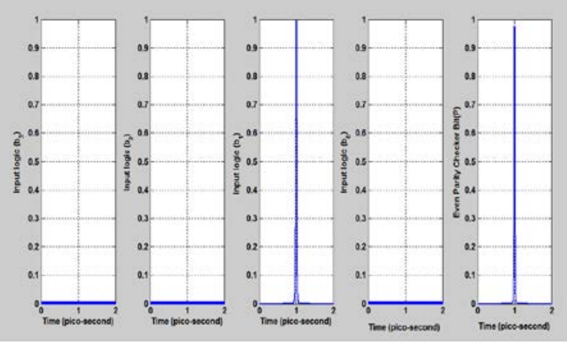

Fig. 6:Simulated result using MATLABfor the proposed 4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0010, which shows the corresponding even parity checker bit as '1'.

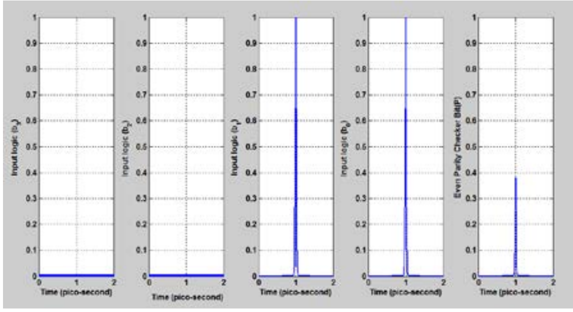

Fig.7: Simulated result using MATLABfor the proposed 4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0011, which shows the corresponding even parity checker bit as '0'.

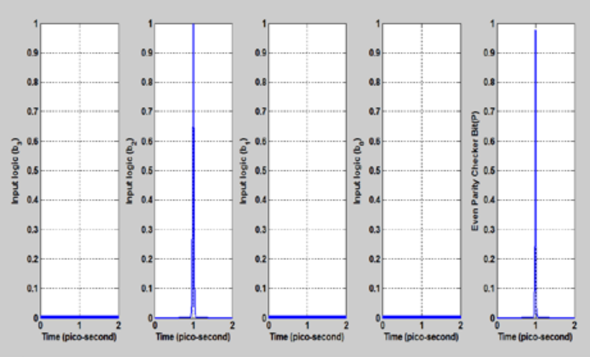

Fig.8: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0100, which shows the corresponding even parity checker bit as '1'.

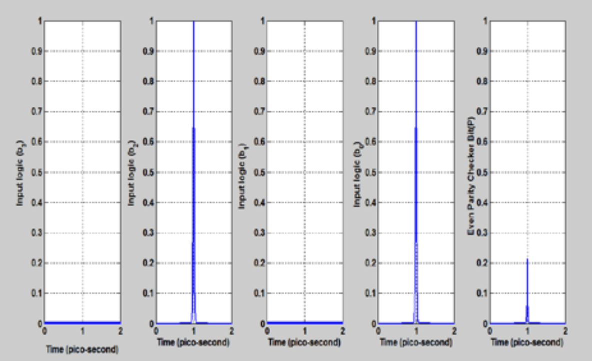

Fig.9: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0101, which shows the corresponding even parity checker bit as '0'.

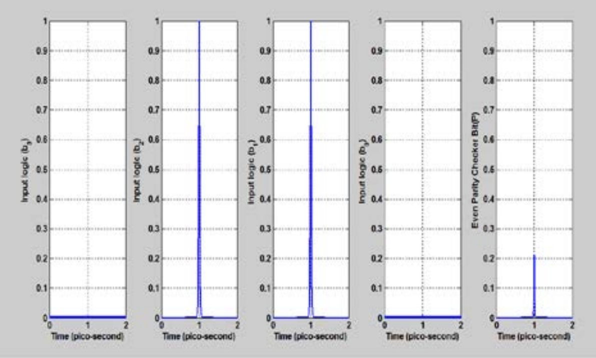

Fig.10: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0110, which shows the corresponding even parity checker bit as '0'.

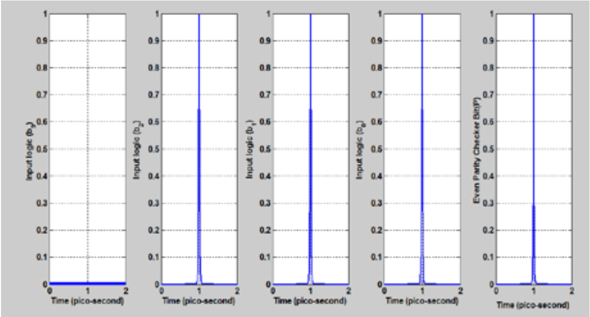

Fig.11:Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 0111, which shows the corresponding even parity checker bit as '1'.

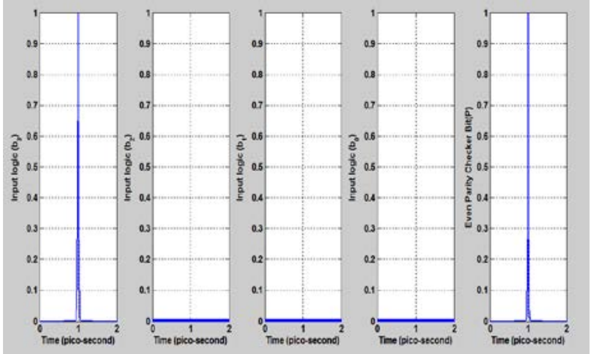

Fig.12:Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1000, which shows the corresponding even parity checker bit as '1'.

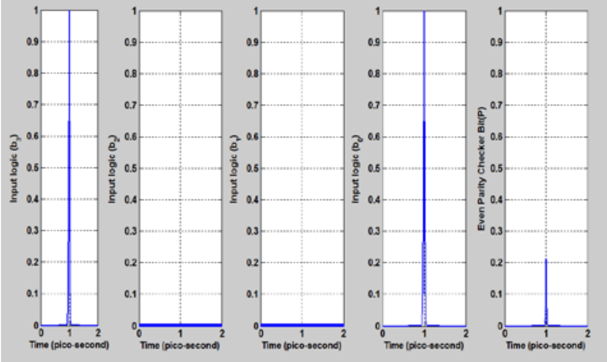

Fig.13: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1001, which shows the corresponding even parity checker bit as '0'.

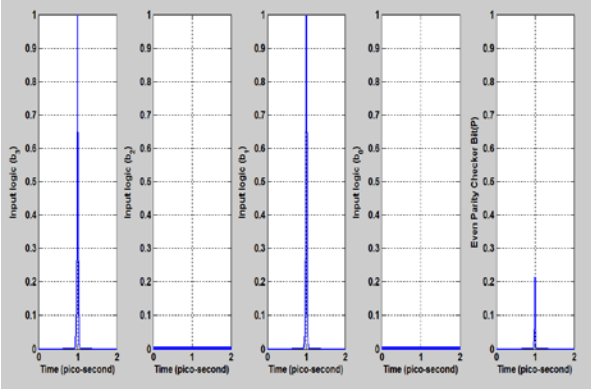

Fig.14: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1010, which shows the corresponding even parity checker bit as '0'.

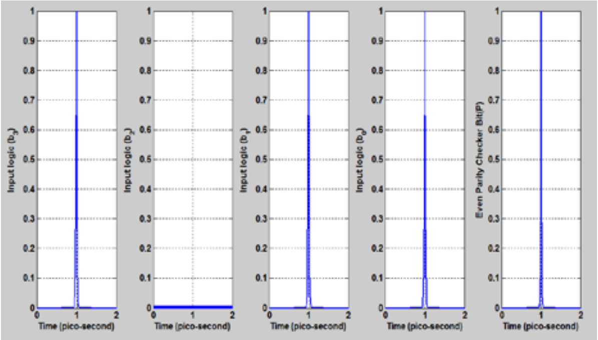

Fig.15Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1011, which shows the corresponding even parity checker bit as '1'.

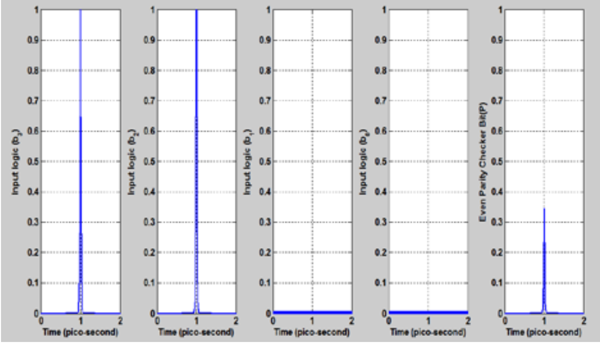

Fig.16: Simulated result using MATLABfor the proposed 4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1100, which shows the corresponding even parity checker bit as '0'.

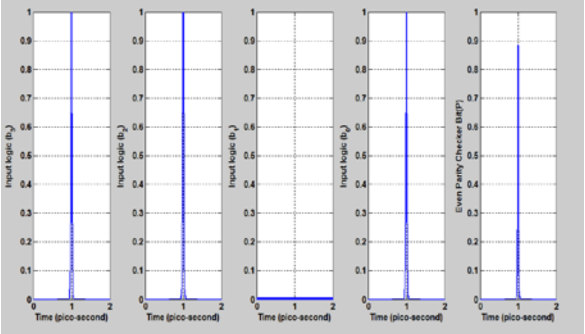

Fig.17: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1101, which shows the corresponding even parity checker bit as '1'.

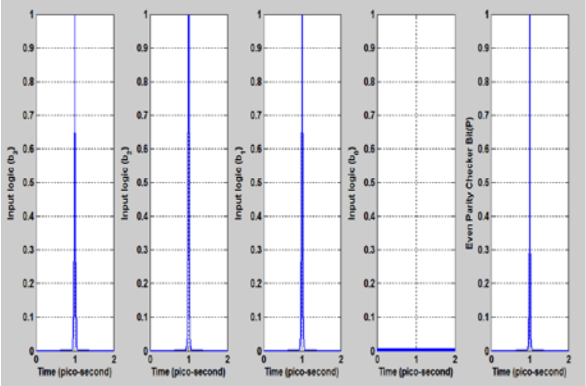

Fig.18: Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0$ → 1110, which shows the corresponding even parity checker bit as '1'.

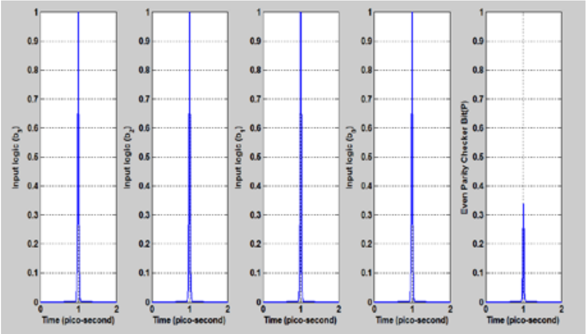

Fig.19Simulated result using MATLABfor the proposed4 bit even parity checker for the input bit sequence $b_3b_2b_1b_0 \rightarrow 1111$, which shows the corresponding even parity checker bit as ‘0’.

Figure 4-19 shows the suitability of the proposed MRR based 4-bit even parity checkers. In the figs 4-19, the first 4 figure represents the different combination of optical input bit sequences $b_3b_2b_1b_0$, where the bit sequences acquire the value from $0000 \rightarrow 1111$. The fourth column in each fig. 4-19 describes the corresponding optical equivalent of even parity checker bit.

CONCLUSION

The paper shows some useful application of the MRRstructure to implement the all-optical even parity checker. In the paper, we have represented a detailed discussion about the single MRRarrangement with all the device and simulation parameters. The proper structure of the optimum number of MRRarrangement provides the layout of the proposed even parity checker. It also includessimulated results using MATLAB, which are verified by the conventional truth table of the respective optical digital circuits. The paper involves some optimistic approach to implement some digital circuits e.g. 4-bit even parity checker in the domain of optical communication. Finally, the discussed scheme includes some considerable advantages of the optical communications e.g. miniature size, securesignal transmission, greater bandwidth, etc. Hence, the proposed scheme can be preferable in the field of ultra-speed modern communication systems.

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