Performance Optimization of Digital Circuits using PTL and CMOS Technology

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Abstract

The objective of this research paper is to analyze the various combinational circuit using PTL technology as well as CMOS technology. It mainly focuses on the characteristics of both the logic designs in terms of the power consumption, power supply, power dissipation and chip area. All the combinational and sequential circuits are designed using the LTSpice tool along with their layout designs using the MAGIC layout tool. Hence, all the circuits are analyzed using open-source simulators.

Keywords: - *Adders, Flip flop, PTL, CMOS, Power consumption, Power dissipation, Power supply and Chip area.*

INTRODUCTION

A. Combinational Circuits

Combinational circuits are basically comprised of a variety of logic gates. Logic gates are the fundamental components that can be found in many circuits. They do not contain any memory. Their output depends on the input at that specified time.[2]

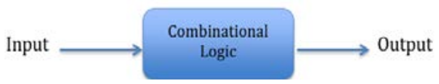

Fig. 1: Block Diagram for Combinational Circuits [2]

B. Sequential Circuits

Sequential logic is a kind of logic circuit whose output depends on the present value of its input as well as on but on past inputs. The sequential logic contains memory, and the elementary memory component is a flip-flop. They are of two types, i.e.:

- Synchronous
- Asynchronous

Sequential logic uses to build finite state machines. FSM is a mathematical model of computation. FSM are of two types:

- Deterministic
- Non-deterministic[3]

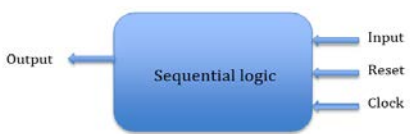

Fig. 2: Block Diagram for Sequential Circuits [3]

C. Pass Transistor Logic (PTL)

Pass transistor logic actually benefits in integrated circuits. It lowers the count of transistors used to create a variety of logic gates by removing unnecessary transistors. To pass logic levels between nodes of a circuit, transistors are used as switches, rather than that switches connected directly to supply voltages.[4]

D. Complementary Metal Oxide Semiconductor (CMOS)

The technology that is used to construct the ICs. These are present in many applications like batteries, microprocessors and etc. They are of two types:

1. N-type CMOS
2. P-type CMOS

In N-type CMOS, there is the presence of electrons in considerable amount than holes, and in P-type CMOS, there are holes in considerable amount than electrons. CMOS transistors are recognized for their effective use of electrical power. They don’t need current except when they interchange one state to another. In addition, the CMOS’s task is to limit the output voltage. The consequence of limiting the voltage is a low-power design that dissipates the least heat. [3]

DESIGNING TECHNIQUES

A. Half Adder using PTL

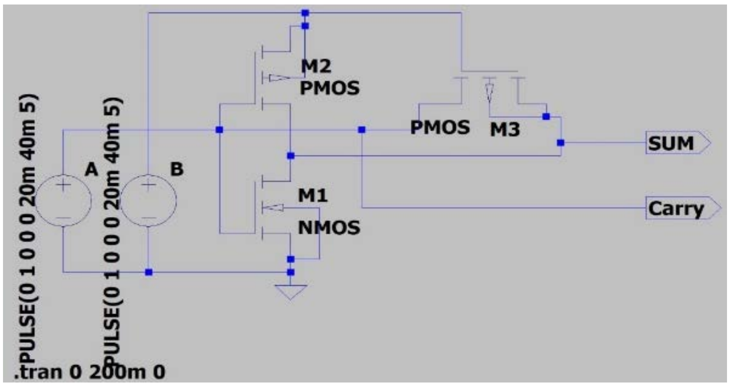

Fig. 3: Circuit Diagram for Half Adder using PTL

Schematic designed from LTSpice for Half Adder using Pass Transistor Logic is shown in Fig. 3.

B. Half Adder using CMOS

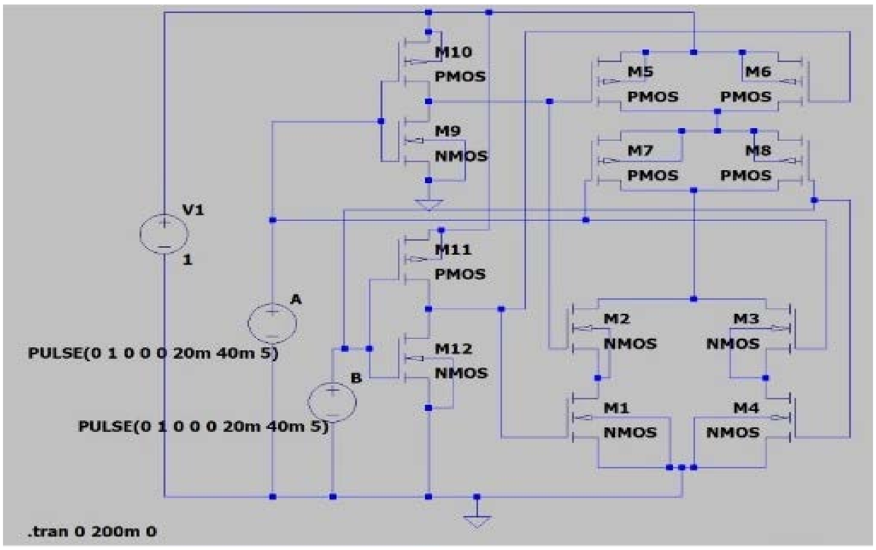

Fig. 4: Circuit Diagram for Half Adder (SUM) using CMOS

Schematic designed from LTSpice for Half Adder (SUM) using CMOS Logic is shown in Fig. 4.

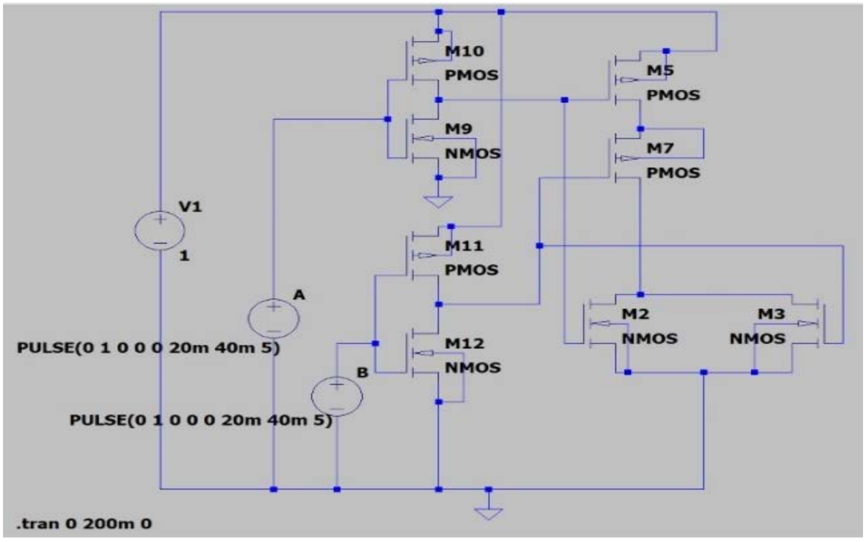

Fig. 5: Circuit Diagram for Half Adder (CARRY) using CMOS

Schematic designed from LTSpice for Half Adder (CARRY) using CMOS Logic is shown in Fig. 5.

C. Full Adder using PTL

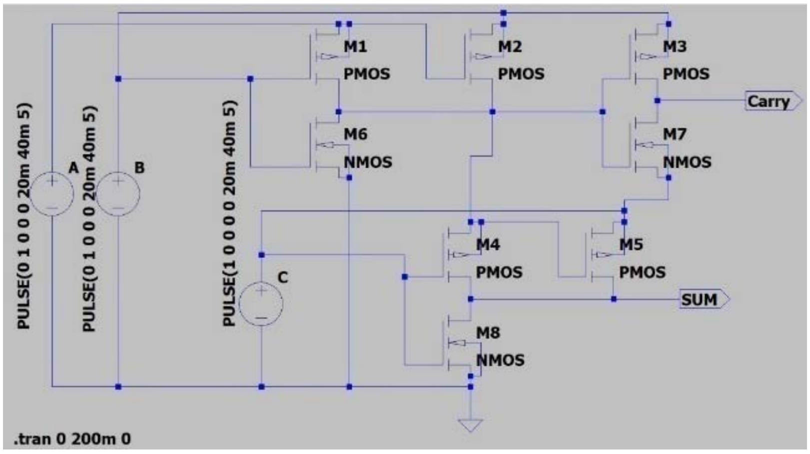

Fig. 6: Circuit Diagram for Full Adder using PTL

Schematic designed from LTSpice for Full Adder using Pass Transistor Logic is shown in Fig. 6.

D. Full Adder using CMOS

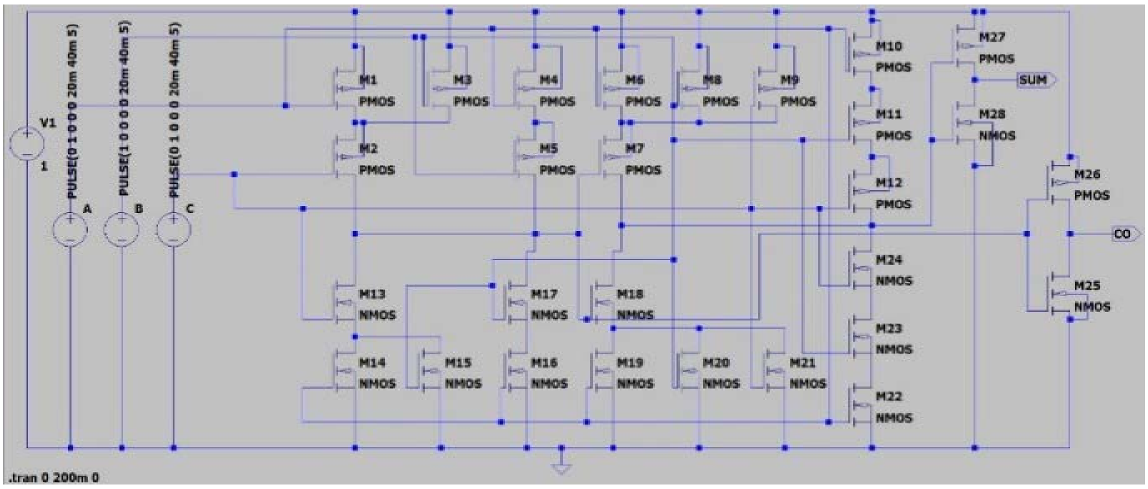

Fig. 7: Circuit Diagram for Full Adder using CMOS

Schematic designed from LTSpice for Full Adder using CMOS Logic is shown in Fig. 7.

E. D flip-flop

A frequently used D flip-flop, also known as "data," or "delay." The D flip-flop catches the D-input value at a given portion of the clock cycle (such as the clock's rising edge). The value captured is the output Q. Sometimes, no improvement in output Q. The D flip-flop can be interpreted as a memory cell, a hold for zero-order or a line for delay [5].

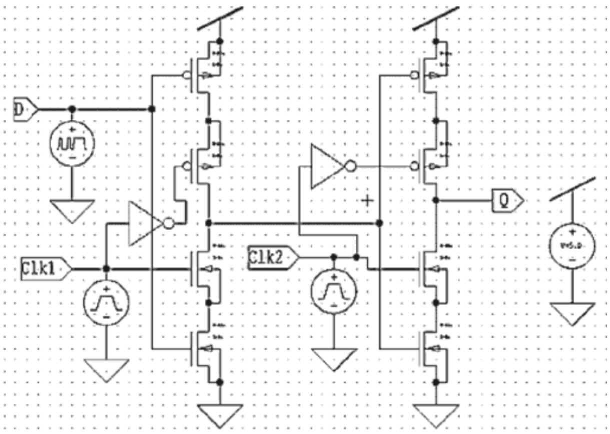

Fig. 8: Circuit Diagram for D Flip Flop using CMOS

RESULT AND COMPARATIVE ANALYSIS

LTspice is a freeware software program running a SPICE electronic circuit simulator, engendered by Linear Technology, a semiconductor maker. It is used in-house for IC design at Linear Technology and the industry's most widely distributed and used SPICE software. To limit its ability, LTspice isn't physically disabled.

The waveform generated from the LTSpice tool is shown in Fig. 9 for Half Adder using PTL.

A. Waveform of Half Adder using PTL

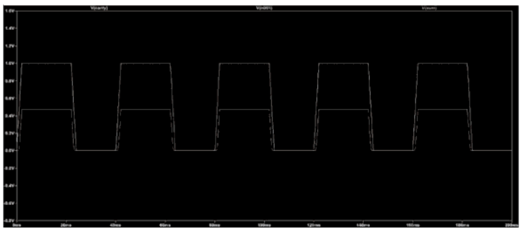

Fig. 9: Waveform for Half Adder using PTL

B. Half Adder using CMOS Waveform

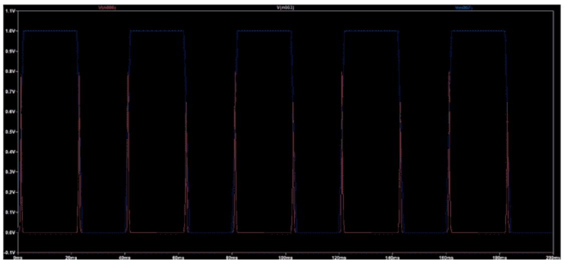

Fig. 10: Waveform for Half Adder (SUM) using CMOS

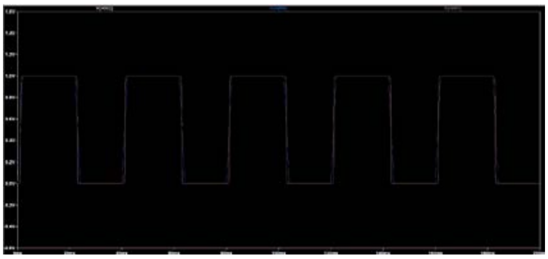

Fig. 11: Waveform for Half Adder (CARRY) using CMOS

The waveform generated from the LTSpice tool is shown in Fig. 10 and Fig. 11 for Half Adder using CMOS.

C. Full Adder using PTL Waveform

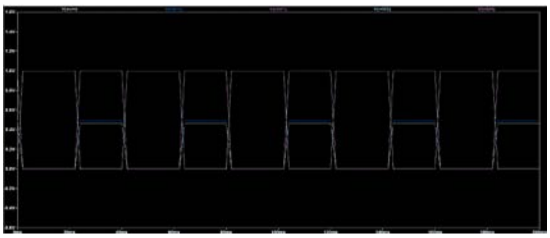

Fig. 12: Waveform for Full Adder using PTL

The waveform generated from the LTSpice tool is shown in Fig. 12 for Full Adder using PTL.

D. Full Adder using CMOS Waveform

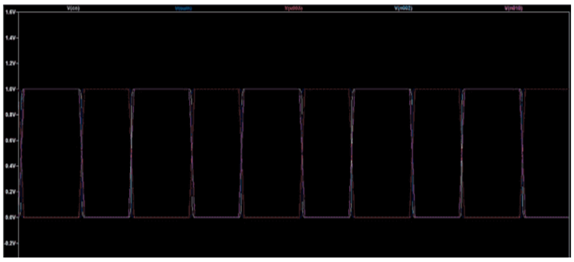

Fig. 13: Waveform for Full Adder using CMOS

The waveform generated from the LTSpice tool is shown in Fig. 13 for Full Adder using CMOS.

E. D Flip-Flop Waveform

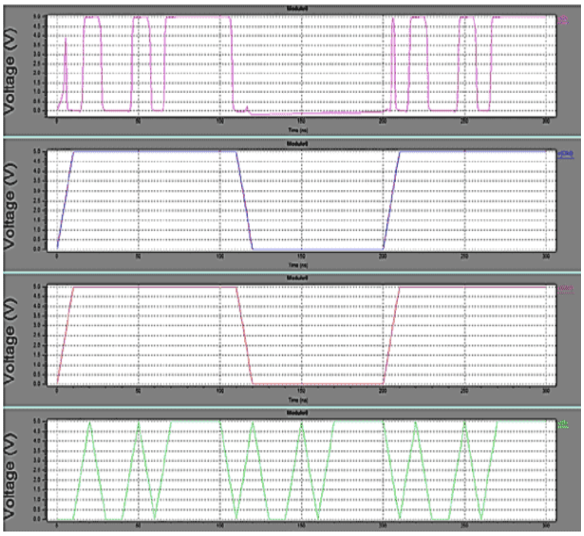

Fig. 14: Waveform for D Flip Flop using CMOS

Fig.14 shows the simulated waveform for D Flip Flop using CMOS. This simulation includes a clock, input pulse and output pulse, respectively.

CONCLUSION

In this paper, it was concluded that the number of transistors used in the design of combinational and sequential circuits such as half adder, full adder and D flip flop using Pass Transistor logic is less compared to conventional CMOS, as well as the delay and average power consumption generated by the PTL predicted half adder, full adder and D flip flop is lower with veneration to conventional CMOS. Power and delay increased, but the transistor count has reduced in HA (half-adder), (FA) full adder, and D- flip flop in pass transistor logic as opposed to traditional CMOS. Therefore, as compared to CMOS logic technology, one can use PTL Technology as better technology for VLSI Power Optimized Circuit Design.

REFERENCES

1. K. D. Shinde and J. C. Nidagundi, "Design of fast and efficient 1-bit full adder and its performance analysis," 2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), Kanyakumari, 2014, pp. 1275-1279.
2. Zimmermann, R., & Fichtner, W. (1997). Low-power logic styles: CMOS versus pass-transistor logic. IEEE Journal of Solid-State Circuits, 32(7), 1079–1090.
3. Kumar, P., Bhandari, N. S., Bhargav, L., Rathi, R., & Yadav, S. C. (2017). Design of low power and area efficient half adder using pass transistor and comparison of various performance parameters. 2017 International Conference on Computing, Communication and Automation (ICCCA).
4. Verma, M. Ramachandran and S. Prince, "Performance analysis for different data-rates of proposed all-optical half-adder and full-adder design," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, 2016, pp. 0114-0118.
5. Mukherjee, B. Roy, A. Biswas and A. Ghosal, "Design of a low power 4×4 multiplier based on five transistor (5-T) half adder, eight transistor (8-T) full adder & two transistor (2-T) AND gate," Proceedings of the 2015 Third International Conference on Computer, Communication, Control and Information Technology (C3IT), Hooghly, 2015, pp. 1-5.
6. S. Srikanth, I. T. Banu, G. V. Priya and G. Usha, "Low power array multiplier using modified full adder," 2016 IEEE International Conference on Engineering and Technology (ICETECH), Coimbatore, 2016, pp. 1041-1044.