

# Simulation and Performance Analysis of Cascode Amplifiers in 90nm and 45nm Technology

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## Abstract

*This paper presents the simulation of differential cascode amplifier, two-stage cascode amplifier and folded cascode amplifier in 90nm & 45nm, and its comparative review study with reported results. Cascode amplifiers render essential output impedance and diminish the impact of miller capacitance, thereby improving speed achievement. In this work, the performance parameters are optimized by respecting their tradeoffs, and the work aims at bandwidth enhancement. The bandwidth is raised by improving trans conductance and lowering the output capacitance. Here the circuit is simulated using cadence virtuoso tool and in gpdk technology. Amongst amplifiers simulated in this paper, the differential cascode amplifiers deliver well in terms of gain, and the folded cascode amplifiers manifest the best speed characteristics. The two-stage cascode amplifiers perform reasonably in terms of gain and frequency. The optimized simulation of differential cascode amplifiers in 45nm manifests 36 dB gain, 15.8 MHz bandwidth, 300 MHz unity-gain bandwidth, and consumes very less power of 195nW. The two-stage cascode amplifier in 45nm exhibits 24.8 dB gain, 950MHz bandwidth and 6.5 GHz unity-gain bandwidth and these values prove the significance of the circuit in high- frequency applications. The folded cascode amplifier in 45nm results in frequency response with 3 dB frequency of 4.9 GHz and UGB of 18GHz. This value shows that the speed performance of folded cascode amplifier in 45 nm is superior over other simulated cascode amplifiers presented in this work and that reported in [1]. The simulated folded cascode amplifier in 45 nm consumes an area of  $2.65\mu\text{m} \times 2.65\mu\text{m}$  ( $7.03 \mu\text{m}^2$ ). It consumes  $67\mu\text{W}$  from a 1V power supply.*

**Keywords:** - Folded Cascode Amplifier (FCA), Two Stage Cascode Amplifier (TSCA), Differential Cascode Amplifier (DCA), Unity Gain Bandwidth (UGB).

## INTRODUCTION

As CMOS technology proceeds, the supply voltage and transistor length shrinks and power dissipation decrease with the cost of complex concerns in the design. A single-stage CMOS amplifier cannot give desired dc voltage gain, output resistance and transconductance. To obtain desired performance, two or more stages of MOS devices are cascaded, and such can provide desired better performance as per stages. Operational Amplifiers are an indispensable part of many analog and mixed-signal systems. Op-amps with several complicated functions are used to realize functions extending from dc bias generation to high-speed amplification or filtering. There are several implementation artifices for

operational amplifiers. Cascode version is one before-mentioned method which is described in [1], and it reveals meaningful advances in performance parameters. The cascode topology is achieved by establishing a common gate stage in series with a common source stage. A cascode sequence introduces input-output separation as there is no direct coupling from the output to input. This connection eliminates the miller effect, and this offers an immensely larger bandwidth. Two or more stages of cascode amplifiers coupled to create a multistage configuration, and it gives better performance features compared to the single-stage structure. In a differential cascode circuit, a cascode current source load is employed to increase gain, and its performance is excellent

in terms of gain and lacks performance in the common-mode range. Folded cascode op-amp concept is a modified cascode structure that offers higher dc gain, high output resistance, better ICMR and PSRR compared to a normal two-stage cascode circuit.

An operational amplifier is a dc-coupled electronic voltage amplifier with a differential input and a single-ended output. In [2], they suggested a source buffered concept to deliver higher EMI immunity over a wide range of frequency from 10 MHz to 1 GHz. That is, this circuit manifests less susceptibility to EMI even in the proximity of substantial amplitude interruptions. In this work, the circuit causes output offset voltage less than 8mV over a wide range of frequencies against a 3.3V peak to peak voltage EMI signal at its non-inverting input. The replica folded cascode amplifier shows a lower output offset voltage than the folded cascode amplifier at all frequencies. An ultra-low supply voltage folded cascode OTA, which operates at 1V supply, is described in [3], and it exhibits a .3V overlap in the permitted input common-mode range, output voltage range and got a dc gain of 69 dB and 2 MHz bandwidth.

An improved fully differential folded cascode op-amp topology presented in[4] achieves an improved dc gain and common-mode rejection ratio without sacrificing slew rate. An alteration to the conventional folded cascode transconductance amplifier is recommended in [5]. It has the benefit of achieving a given set of design specifications by consuming a fraction of power and low voltage. Two-stage recycling folded cascode operationaltransconductance amplifier engaging Gm-C compensation technique proposed in[6] consists of recycling structure, positive feedback and feed-forward compensation path. This work shows better frequency response, CMRR and speed without negatively affecting input-referred noise. The folded cascode OTA concept in [7] embraces extra load branches in parallel, and it improves bandwidth and phase margin by compromising with DC gain and UGB.N. The recycling amplifier reuses[8] existing devices and currents to perform an additional task. The idea of using a push-pull configuration for the input stage of a folded cascode OTA to enhance gain and UGB is discussed in [9].This paper analyses the variation of gain with a parameter K, where K is the ratio of currents of two input NMOS devices to that of cascode transistors.

## PROPOSED METHODOLOGY

A multi-stage cascode topology is designed by joining two or more stages of cascode amplifiers

to provide better performance characteristics compared to the single-stage structure. In a differential amplifier, the gain is too low due to ordinary current source load, and it is substituted with a cascode current source load. This replacement forms a differential cascode amplifier, and so the gain is improved with cascode connection.

In a two-stage cascode amplifier, decent speed performance is achieved by loading differential pairs with two PMOS transistors, and it is cascading with a cascode common source stage. In the folded cascode amplifier, a distinct topology of the differential amplifier is connected with the cascode output stage. This circuit provides broadened bandwidth without many deductions in gain. The unity-gain bandwidth is proportional to transconductance and inversely proportional to capacitance which defines the dominant pole[10].

The transconductance is directly proportionate to the aspect ratio of the transistor, and in folded cascode amplifier, the capacitance at the output node determines the dominant pole. The bandwidth can be augmented by extending transconductance and declining output node capacitance. In this work, three different cascoded amplifiers, namely differential cascode, two-stage cascode and folded cascode amplifiers, has been redesigned and simulated in a lower node (90nm & 45nm) to get optimum performance in terms of bandwidth, gain and power. In folded cascode amplifier, higher bandwidth is achieved by adjusting the aspect ratio and thereby its transconductance. At last, the comparative performance analysis has done with recently reported results in terms of simulated results and area.

### A. Differential Cascode Amplifier

The schematic description of the differential cascode amplifier is presented in Fig. 1. In this circuit, a cascode circuit is applied as a load of differential pair. This cascode connection increases gain over the conventional differential amplifier. But positive common-mode voltage is limited due to this cascode part. In the differential cascode amplifier, the gain is enhanced by improving the transconductance of differential transistor pairs.

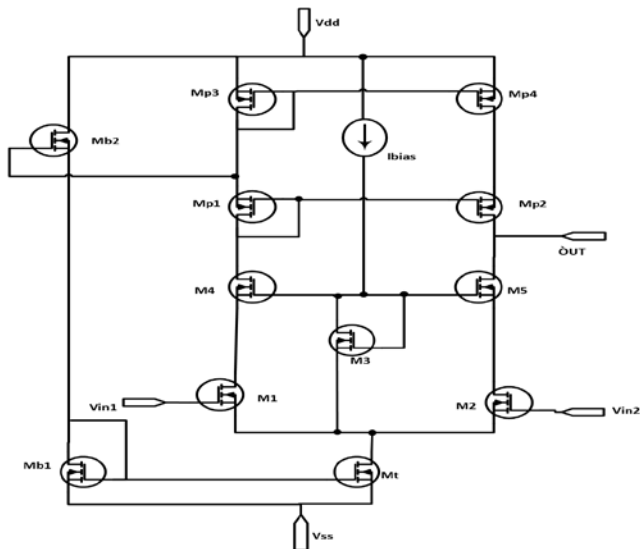


Fig. 1: Schematic of Differential cascode amplifier

### B Two Stage Cascode Amplifier

The schematic description of the two-stage cascode op-amp is presented in Fig.2. In this circuit, the first stage is a differential amplifier with a PMOS load, and it is cascaded with the secondary stage, which is a cascode circuit. The initial stage load formulates a balanced op-amp as the resistances observed from sources of differential pairs are indistinguishable. In this, mirror operation is taking place by which currents are copied and merged at the output to generate the desired voltage gain.

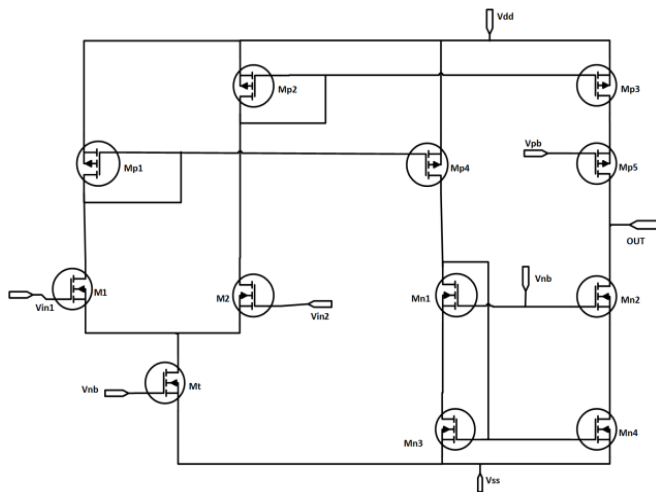


Fig. 2: Schematic of Two stage cascode amplifier

### A. Folded Cascode Amplifier

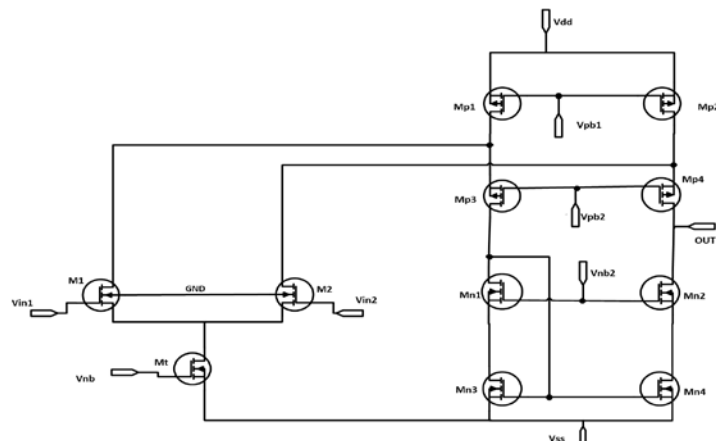


Fig. 3: Schematic of Folded cascode amplifier

The circuit schematic of the folded op-amp is shown in Fig. 3. This topology is utilizing cascode connection in the final stage connected with odd differential amplifier configuration results in good ICMR and gain. There is no necessity for the perfect symmetry of differential amplifier currents since the additional DC can flow into or out of the current mirror. In this work, we are simulating folded cascode amplifier in 45nm and 90nm and comparing the results with reported data in terms of various performance parameters.

**D. Design and Analysis**

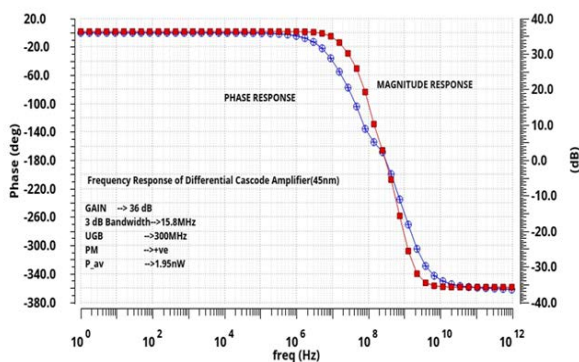
The simulation of cascode amplifiers in 45nm and 90nm and relative study with reported data has been done in this work. The reduced gain performance of the conventional differential amplifier with the current source load is improved by using a cascode current source load in the differential cascode amplifier. The Eqn. 1 gives the gain of the specified circuit, and so the gain can be boosted by enhancing transconductance. [11]

$$A_v = g_{m1} (g_{m2} r_{o2} || g_{m4} r_o) \tag{1}$$

**RESULTS**

In this paper, the differential cascode, two-stage cascode and folded cascode amplifiers were simulated in 90 nm and in 45nm. The simulated results were compared with reported results in [1][6] & [13].

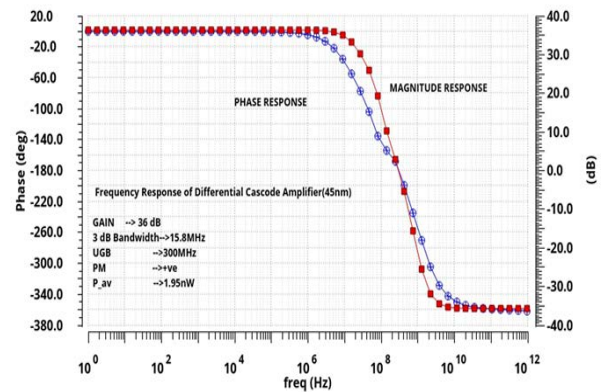
**A. Differential Cascode Amplifier in 90 nm & 45nm**



**Fig. 4: Frequency Response of DCA in 90nm**

The differential cascode amplifier is simulated with a 1V supply, 10nA bias current and in 90nm technology. This simulation manifests 41 dB gain, 90 kHz bandwidth, 5MHz UGB with a power consumption of 4.3uW. In this, the maximum bias current is limited to 110nA. The frequency response of DCA in 90nm is sketched in Fig. 4. The same circuit is then simulated in 45 nm technology under 900mv supply and 120nA bias

current. This simulation exhibits 36dB gain, 15.8MHz bandwidth, 300MHz UGB, and power consumption of 195nW, and it is given in Fig.5.

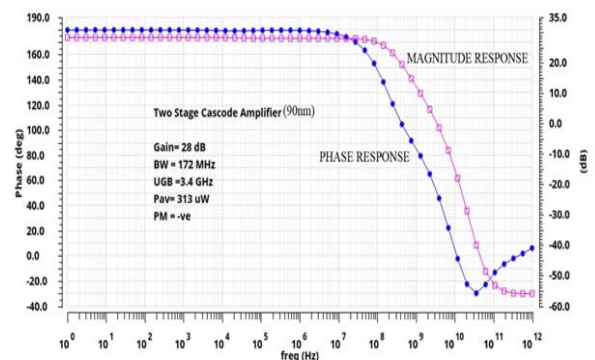


**Fig. 5: Frequency Response of DCA in 45nm**

**B. Two Stage Cascode Op-Amp in 90nm & 45nm**

The two-stage cascode operational amplifier shown in Fig.2 was simulated in 90nm and 45 nm technology with a 1.5V supply. The frequency response of the two-stage cascode amplifier in 90nm and 45nm is shown below in Fig.6 and Fig.7, respectively.

In 90nm simulation, different bias currents have been experimented with and chosen a good result. The simulation with an 8µA bias current presents 29.7dB gain, 116MHz bandwidth, 2.75GHz UGB and 157µW power consumption. The TSCA with 20µA results in 28dB gain, 172 MHz bandwidth, 3.4 GHz UGB with the power consumption of 313µW. The design and simulation of TSCA in 45 nm with 1V supply and 20µA bias current gave 24.76 dB gain, 950MHz bandwidth and 6.5GHz gain-bandwidth product with average power 60µW. In the simulation of TSCA in the same technology with bias current in nA range have been neglected due to insufficient gain.



**Fig. 6: Frequency Response of TSCA in 90nm**

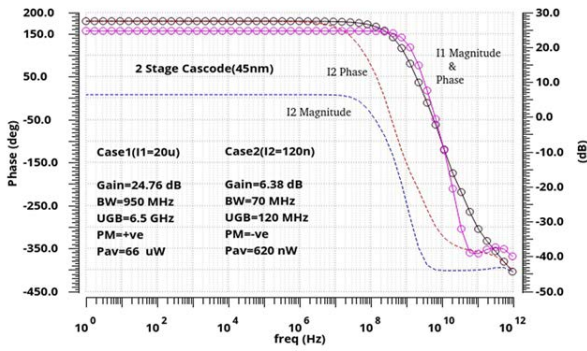


Fig. 7: Frequency Response of TSCA in 45nm

### C. Folded Cascode Op-Amp in 90nm & 180nm

The performance of the folded cascode amplifier is augmented by redesigning the circuit in 90nm and 45nm technology. The circuit is simulated in 90nm, and its frequency response is given in Fig.8. This frequency response presents 31.7dB gain, 989MHz bandwidth, 20GHz gain-bandwidth product and 144uW average power consumption.

The folded cascode amplifier in 45nm technology is simulated with 1V supply voltage and different bias current. The circuit simulation with 8u bias current manifests 23.5dB gain, 1.3GHz bandwidth, 12GHz unity-gain bandwidth and 29.23 uW power consumption. Then the circuit is trialled with a 20u bias current, and both responses are given in Fig.9. The second attempt exhibits 14dB gain, 4.9GHz bandwidth, 18GHz unity-gain bandwidth and 67 uW power consumption. The tradeoff between performance parameters is reflecting in the above results, and the values are taken based on objectives.

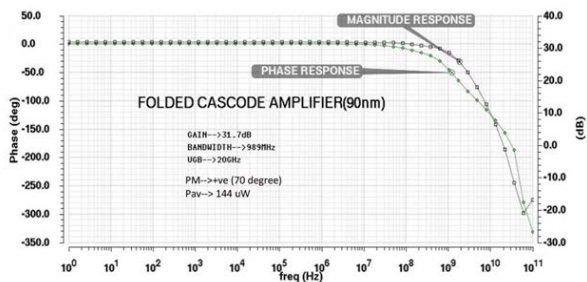


Fig 8: Frequency Response of FCA in 90nm

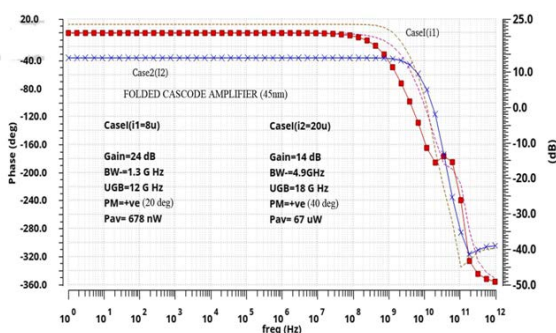


Fig. 9: Frequency Response of FCA in 45nm

### D. Layout

The physical design intends to improve electrical performance. Better matching is more critical in physical design than area effectiveness. After the physical design, three steps have been done. The first step was DRC (Design Rule Check) to check whether the designed layout satisfies all geometric rules or not. The second step is LVS (Layout versus Schematic) to check the matching between the designed circuit and layout and to circumvent defects.

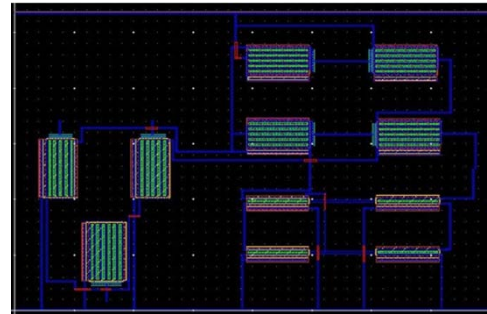


Fig. 10: Layout of FCA in 90nm

In 90nm CMOS technology, as in Fig.10, the folded cascode amplifier layout dimensions were measured as 40.7um, and 26.8um and so the area was 1090.76um<sup>2</sup>. In 45nm CMOS technology, the folded cascode amplifier layout dimensions were measured as 2.65um and 2.65um and the area was 7.03um<sup>2</sup>, which is given in Fig.11.

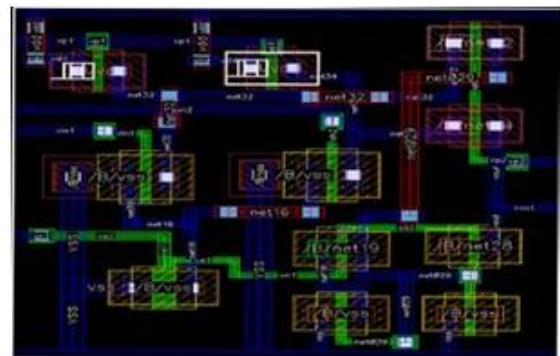


Fig. 11: Layout of FCA in 45 nm

While interpreting the area occupied in both the technologies, it can be concluded that the area corresponding to 45nm technology is less than that of 90nm technology. This point validates the fact that sizing down the device dimensions improves the number of transistors that can be included in a given area.

### E. Performance Analysis

A comparison between differential cascode amplifier, two-stage cascode amplifier and folded cascode amplifier in 45nm, 90nm with reported work in [1] is summarized in Table.1. The design of the differential cascode amplifier (DCA) in 45

nm technology is excellent in terms of power consumption (195nW), and DCA simulation in 90nm is useful in the consideration gain (41dB).

In the case of speed performance and phase margin, the DCA is not suitable compared to the other cascode amplifiers mentioned in this paper. But the design of a two-stage cascode amplifier in 45nm exhibits improved speed performance (950MHz BW & 6.5GHz UGB) compared to the two-stage cascode amplifier reported in [1] (2MHz BW& 10MHz UGB), and TSCA in 90nm (172MHz BW & 3.4GHz). But the poor phase margin shows stability issue in TSCA, and gain is reduced compared to DCA and FCA.

The simulation of folded cascode amplifier in 90nm exhibits very significant advancement in 3 dB bandwidth and unity-gain bandwidth compared to the folded cascode amplifier reported in[1][6][13], and it is about 988MHz and 20 GHz, respectively.

The same circuit in 45nm on the different bias current (8µA/20µA) shows much improvement in 3dB bandwidth and unity-gain bandwidth compared to reported results, and it is about (1.29GHz/4.89 GHz) & (11.99GHz/18.99 GHz) respectively. Even there is a decrease in gain due to a tradeoff among gain and bandwidth, we are getting a response with gain nearly equal to (25dB/15dB), which is not much less, and it can fit in different high-frequency applications.

Compared to differential cascode amplifier and two-stage cascode amplifier, the folded cascode amplifier shows improved stability in terms of phase margin, and it is nearly equal to 60°. The layout simulation has been done (in 45nm & 90nm), and the area occupied was about 7 µm<sup>2</sup>, and it is the optimised area compared to that in 90nm technology. See **Table 1**.

**TABLE.1**Comparative performance analysis with reported results

Topology	Tech.	Gain	BW	UGB	PM	Area	Pav
Unit	nm	dB	Hz	Hz	degree	m <sup>2</sup>	W
TSCA[1]	1250	12	2M	10M	100(+)	-----	<5m
FCA[1]	1250	56	10K	7M	85(+)	-----	<5m
PRFC[6]	180	111	1K	20M	63	.01m	.4m
FCA[13]	45	35.7	25M	978M	81	-----	2.12m
DCA	90	<b>41</b>	90K	5M	16(+)	-----	4.3µ
TSCA	90	28	172M	3.4 G	-ve	-----	313µ
FCA	90	31.7	989M	<b>20G</b>	<b>70(+)</b>	1091µ	144µ
DCA	45	36	15.8M	300M	10(+)	-----	<b>195n</b>
TSCA	45	24.8	950M	6.5G	120(+)	-----	60µ
FCA(I=8µA)	45	<b>23.5</b>	<b>1.3G</b>	<b>12G</b>	16	<b>7.03µ</b>	29.23µ
FCA(I=20µA)	45	14	<b>4.9G</b>	<b>18G</b>	<b>40</b>	<b>7.03µ</b>	67µ

**CONCLUSION**

The differential cascode amplifier, two-stage cascode amplifier and folded cascode amplifier with improved performance were simulated and compared with reported results. The circuit was simulated in gpdk 45nm and gpdk 90nm technologies. The differential cascode amplifier is looking good in terms of gain and power consumption (nW), and its speed performance is not adequate for high-frequency applications. The simulated two-stage cascode amplifier is moderately suitable for high-frequency applications due to its improved bandwidth. The simulation of folded cascode amplifier in 45nm technology results in the 3 dB bandwidth nearly equal to 5GHz, and so the circuit can be used for high- frequency applications. The simulation has been done using the cadence virtuoso tool. The designed cascode circuits operated in 1 V and the power consumption measured was 67µW. The layouts of folded cascode op-amp in both the technologies were prepared, and the area consumption was 7µm<sup>2</sup>. The different topology approaches have experimented with for further improvement in bandwidth, and it is found that the modified common source amplifier as the next stage will improve bandwidth.

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