New Electronic / Resistor Tunable Grounded Inductance Simulation Configuration

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Abstract

In this research communication a novel electronically/resistor adjustable grounded inductance simulation con- figuration has been developed. This design is developed by employing two VDCCs (Voltage Differencing Current Convey- ors) along with three grounded resistances and one grounded capacitance. The developed configuration enjoys advantages like employment of only grounded capacitance and resistance, no need of matched active/passive components, availability of inductance value control through grounded resistances and bias currents (electronic adjustments) of used VDCCs, undeviated performance under non-ideal environment and small passive/active sensitivity index values. The utility of designed synthetic inductance has been validated through a second order band-pass filter designed employing it. To validate the theoretical/mathematical results, simulations in PSPICE environment have been executed employing CMOS based VDCCs.

***Keywords: -** Electronic control, Resistance control, Synthetic inductor, VDCC).*

INTRODUCTION

An inductor is a well-known circuit element which is highly useful in electrical engineering applications. Due to various disadvantageous features such as big size, low quality factor, high losses and harmonic generation, the conventional spiral inductors are not recommended for on-chip electronic systems[27]. Therefore, synthetic active inductors are a good choice for electronic systems. An active synthetic inductor is a circuit configuration which has active element(s), resistor(s) and capacitor and simulates the behavior of a conventional spiral inductor. Additionally, simulation of lossy inductor is found useful along with simulation of lossless inductors. The wide range of application of grounded lossy inductance simulation is filters, sinusoidal oscillator and series/parallel resonance circuits[28]. In the last three decades, several active circuits for implementing the behavior of grounded inductance have been proposed in the open literature [1-18]. On careful study of these previously reported circuits, following conclusions can be drawn.

1. Some configurations employ more than two active elements [1], [3], [4], [5], [8].
2. A number of circuits employ floating resistors and/or floating capacitance which is not an advantageous feature from the view-point of efficient chip area utilization [2], [3], [5-9], [11], [13], [14], [15]
3. Some implementations do not have the facility of electronic adjustment of simulated inductance [1-9], [11-14].
4. Some configurations simulate lossy inductance in non- ideal environment [1], [3], [4], [6], [7], [9], [10], [13], [15].
5. Some designs have component matching constraints [4], [6], [7], [9], [11], [13], [15].
6. Some circuits employ two capacitances which makes the circuit oversized as for an inductance simulation, a single capacitance is sufficient [16-18].

Therefore, this work aims to design an active synthetic inductance simulator which is developed by employing two VDCCs, single grounded capacitance and three resistances (all grounded). As all four external passive components are grounded, the circuit is found appropriate for monolithic development. The reported structure enjoys inductance value tuning through grounded

resistances (resistance tuning) and VDCC bias current tuning (electronic tuning). The proposed configuration simulates the behavior of lossless inductor in ideal as well as non-ideal conditions without any need of active/passive component matching.

VDCC CIRCUIT IDEA

The VDCC is a very popular circuit idea firstly reported in [19]. The single block level depiction of conventional VDCC is illustrated in Fig.1 and its CMOS realization in shown in Fig.2[20]. The VDCC consists six current/voltage ports in which all the terminals are at high impedance level excluding the terminal 'X'. The voltage-current relations among various ports of a VDCC can be illustrated by equation set (1), which confirm the current mode, voltage mode, and trans conductance mode operations of VDCC.

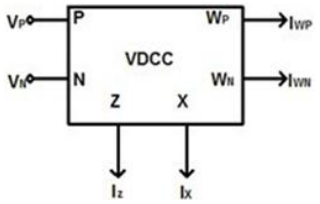

Fig. 1: Single block symbol of conventional VDCC

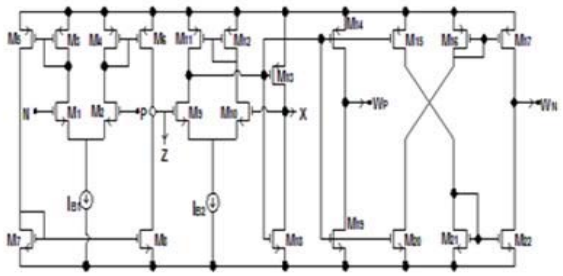

Fig. 2: Popcular realization of VDCC element employing CMOSs

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (1)$$

Where 'gm' is input stage transconductance gain of VDCC.

In recent past, several circuits using VDCC(s) in analog electronics were proposed in [21-26].

PROPOSED CONFIGURATION

The developed synthetic active inductance simulation configuration employing VDCCs is illustrated in Fig.3.

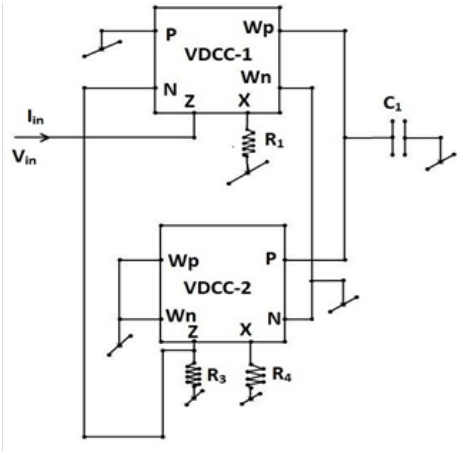

Fig. 3: Proposed synthetic grounded inductor

By simple circuit analysis of configuration given in Fig.3, the impedance of this can be evaluated as

$$Z_{in} = \frac{V_{in}}{I_{in}} = s\left(\frac{R_1 C_1}{R_3 g_{m_1} g_{m_2}}\right) = sL_{eq} \quad (2)$$

$$\text{Where, } L_{eq} = \frac{R_1 C_1}{R_3 g_{m_1} g_{m_2}} \quad (3)$$

Here gm1 and gm2 correspond to the trasnconductance of VDCC-1 and VDCC-2 respectively.

The expression (2), clearly reflects that the configuration of Fig.3 simulates the behavior of grounded inductor with inductance value 'Leq'. The simulated inductance 'Leq' can be adjusted by resistances R1/R2. Therefore, the circuit exhibit the facility of grounded resistance control. Similarly, by varying gm1/gm2, we can also adjust the value of 'Leq' which is termed as electronic adjustment of 'Leq'.

NON IDEAL STUDY

On taking non-ideal mathematical model of VDCC under consideration, the current-voltage equations are given in Eq. (4),

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{wp} \\ 0 & 0 & 0 & -\gamma_{wn} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (4)$$

Here γ, β and α are non-ideal current transfer error, non-ideality correspond to voltage and transconductance error respectively. In the ideal case, we assume all these values equal to unity, but in non-ideal conditions, these values are slightly less than 1. On revisiting the configuration reported in Fig.3, using equations at (4), the input impedance can be evaluated as

$$Z_{in} = \frac{V_{in}}{I_{in}} = s\frac{R_1C_1\beta_1\beta_2}{\alpha_1\alpha_2 g_{m1}g_{m2}\gamma_{\omega P_1}R_3} = sL_{eq1} \qquad (5)$$

Where $L_{eq1} = \frac{R_1C_1\beta_1\beta_2}{\alpha_1\alpha_2 g_{m1}g_{m2}\gamma_{\omega P_1}R_3}$ (6)

Where α_1, α_2 are transconductance error, β_1, β_2 are non-ideality for voltage of VDCC1 and VDCC2 respectively and $\gamma_{\omega_{P_1}}$ is error in transfer of current of VDCC1.

So, it is clearly understood, through Eq. (5), that on considering non ideal limitations, the presented configuration realizes the behavior of a loss-less inductor of inductance value 'Leq'. As the circuit is still working like a lossless inductor, we can say that the working of the proposed configuration does not get affected by non-ideal constraints and the value of realized inductance 'Leq' is very slightly less than ideal state value 'Leq'.

The sensitivities of realized inductance, 'Leq' for different passive element values and active parameters can be found as

$$S_{\beta_1}^{L_{eq1}} = 1, S_{\beta_2}^{L_{eq1}} = 1,\ S_{\alpha_1}^{L_{eq1}} = -1,\ S_{\alpha_2}^{L_{eq1}} = -1,$$

$$S_{\gamma_{\omega p1}}^{L_{eq1}} = -1, S_{g_{m_1}}^{L_{eq1}} = -1, S_{g_{m_2}}^{L_{eq1}} = -1, S_{R_1}^{L_{eq1}} = 1$$

$$S_{C_1}^{L_{eq1}} = 1, S_{R_3}^{L_{eq1}} = -1\,,\ S_{R_4}^{L_{eq1}} = 0 \qquad (7)$$

From Eq. (7), we can see that the magnitudes all sensitivity indexes are not more than one.

APPLICATION EXAMPLE

The usefulness of the developed inductance simulation circuit can be demonstrated by designing a second order voltage mode bandpass filter. The conventional passive RLC bandpass filter employing grounded inductor is given in Fig.4. On replacing inductor of Fig.4 by developed synthetic inductor, an active bandpass filter is constructed which is shown in Fig.5

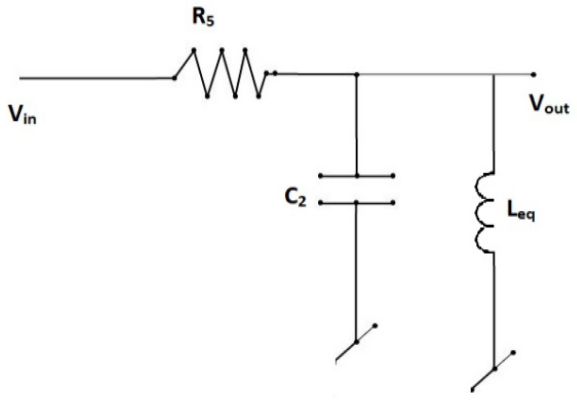

Fig. 4: Conventional RLC Band-pass Filter

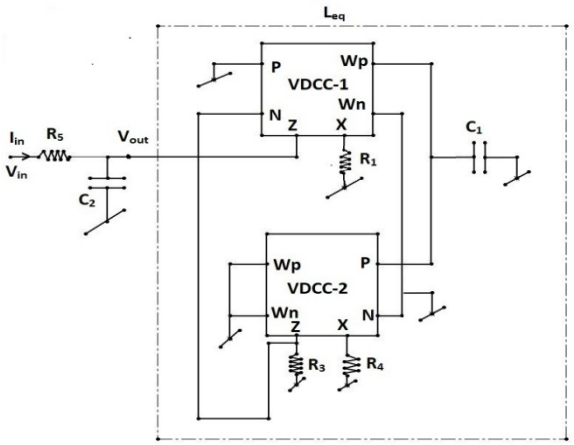

Fig. 5: Active implementation of filter shown in Fig.4 employing designed inductor simulator.

The active implementation of filter connection depicted in Fig.4 is demonstrated byFig.5 by removing passive resistance by placing presented Inductor simulator in grounded resistance mode.

SIMULATION RESULTS

For validation of reported circuits, the PSPICE simulations have been performed including CMOS based VDCCs (given in Fig.2). For simulation study of developed design given in Fig.3, the active/ passive component values are taken as: R1=R3=R4=1KΩ, C1=0.1nF with supply voltages ±0.9V DC and bias current values Ib1=50µA (for both the VDCCs) and Ib2=100µA (for both the VDCCs).

The software simulated magnitude/phase response curves of input impedance have been plotted in Fig.6 and Fig.7, which confirm the working of developed circuit as grounded inductor.

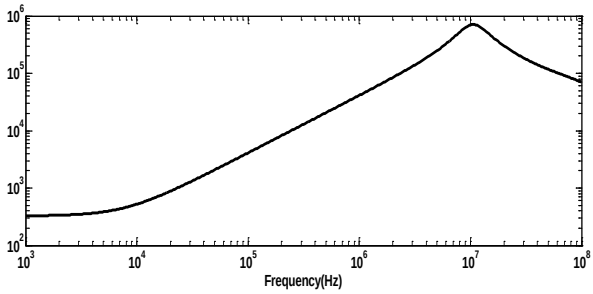

Fig. 6: Magnitude Vs frequency plot of input impedance of configuration shown in Fig.3

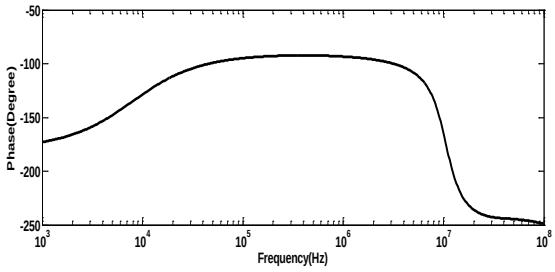

Fig. 7: Phase Vs Frequency plot of input impedance of configuration shown in Fig.3

The variations in realized inductance on choosing different values of capacitance C1(keeping R1=R3=R4=1KΩ and bias currents Ib1=50µA and Ib2=100µA) are shown in Fig.8. Also, the resistor tuning of realized inductance through grounded resistance R1(keeping R3=R4=1KΩ and bias currents Ib1=50µA and Ib2=100µA) in demonstrated in Fig.9.

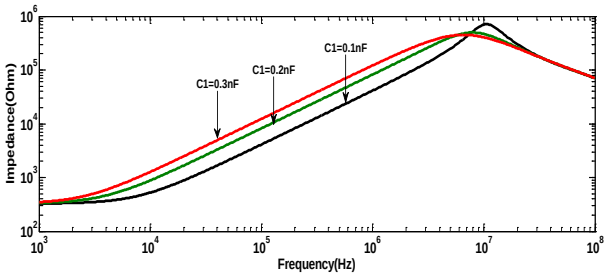

Fig. 8: Effect of capacitance (C1) variation on input impedance.

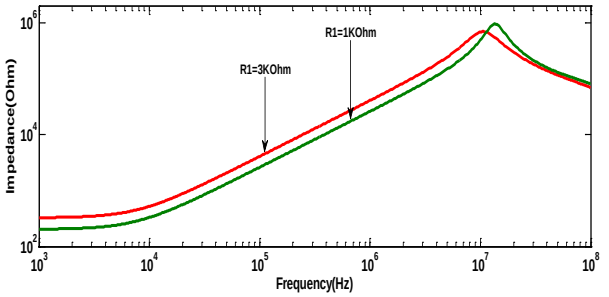

Fig. 9: Resistor tuning through resistance R1

Similarly, the electronic variability of developed inductance using Ib1(Biasing current) of both the VDCCs (Ib1=50µA, 100µA, 150µA) keeping Ib2 for both VDCCs at 50µA, is shown in Fig.10.

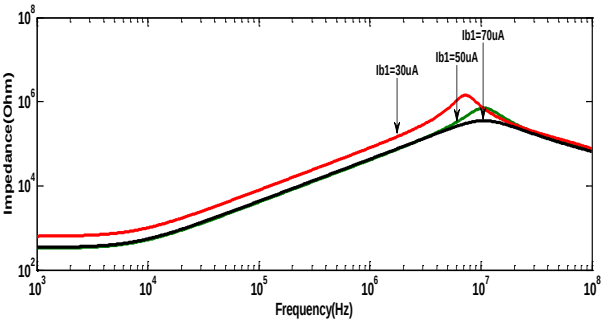

Fig. 10: Electronic tuning through Ib1 of both the VDCCs

The performance of application filter developed in Fig.5 is also studied by simulations with passive elements values. The simulation plot of frequency vs gain characteristics shown in Fig.5 is provided in Fig.11.

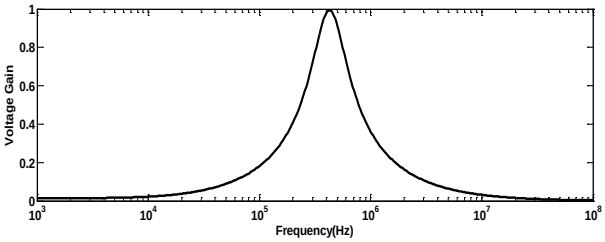

Fig. 11: Frequency response of filtering circuit given in Fig.5

CONCLUSION

A novel active grounded inductance simulation configuration is reported. The proposed design has two VDCCs with four passive components, all connected to ground. The circuit has many advantages like as the empolyment of all passive elements in grounded state, availability of electronic/resistor adjustment, no matching components requirements, working is satisfactory with small sensitivities for non-ideal considerations. The PSPICE simulations were used to verify theoretical as well as mathematical analysis.

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